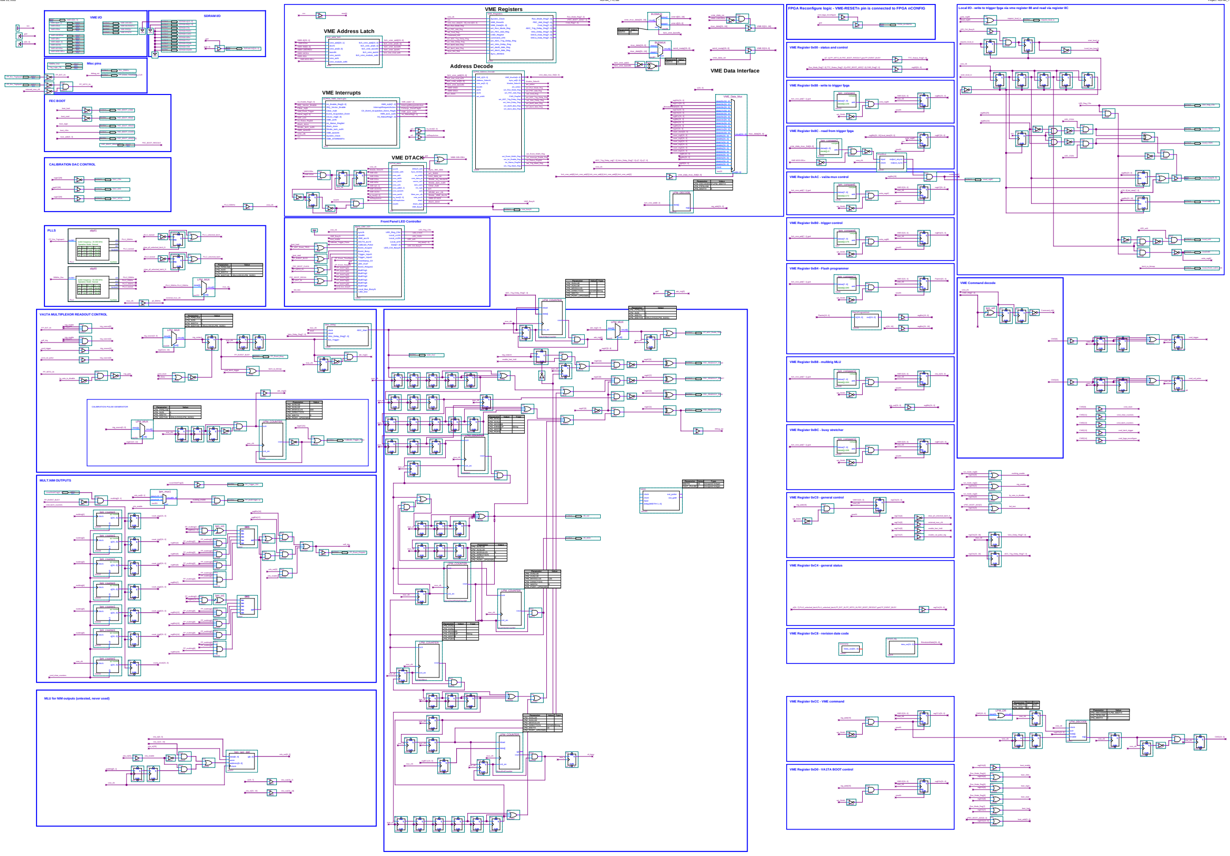
VME I/O
SDRAM I/O
Misc pins
FEC BOOT
CALIBRATION DAC CONTROL
PLLS
VME Address Latch
VME Registers
Address Decode
VME Interrupts
VME DTACK
VME Data Interface
Front Panel LED Controller
VA1TA MULTIPLEXOR READOUT CONTROL
MULTI-MM OUTPUTS
MLU for NIM outputs (unlocked, never used)
FPGA Reconfigure logic - VME-RESET* pin is connected to FPGA nCONFIG
VME Register 0x00 - status and control
VME Register 0x08 - write to trigger fifo
VME Register 0x0C - read from trigger fifo
VME Register 0x1C - va1ta mux control
VME Register 0x80 - trigger control
VME Register 0x84 - Flash programmer
VME Register 0x88 - multibg MLU
VME Register 0x8C - busy stretcher
VME Register 0xC0 - general control
VME Register 0xC4 - general status
VME Register 0xC8 - revision date code
VME Register 0xCC - VME command
VME Register 0xD0 - VA1TA BOOT control
Local IO - write to trigger fifo via register 08 and read via register 0C
VME Command decode