SIS3801
VME Multiscaler

User Manual
for Firmware V5 through VE

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Revision Table:

Revision	Date	Modification
1.0	22.01.99	Generation from SIS3801 standard manual remove broadcast functions reduced copy disable register add internal LNE pulser and LNE prescaler
1.1	26.01.99	FIFO flag changes V2/V3 PAL
1.11	29.01.99	bug fix in control register default settings
1.12	12.02.99	bug fix in status register (IRQ source)
1.20	23.06.99	V7, V8 LNE inhibit input modes added
1.21	13.07.99	V7, V8 enable external LNE in control register added
1.30	17.04.00	V9, VA LNE prescaler extension to 28-bits
1.31	29.05.00	FIFO VME access D32/BLT32 fix
1.32	28.08.00	LNE Prescale factor reload procedure added
1.40	29.03.01	Version 0xB and 0xC, RORA/ROAK IRQ style selectable via
1.50	30.11.12	Version 0xD and 0xE, - reduced the programmable length of the IRQ Vector from 8 bits to 2 bits (bits 7 to 2 are 0) - reduced bit width of "Copy Disable" register from [24:0] to [17:0] - add 19-bit "Acquisition Count" register (read only) - add 18-bit "Acquisition Preset" register (write only)

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1   Introduction

The SIS3801 is one of the multi channel scaler (multiscaler) boards of the SIS360x/38xx VMEboard family. The SIS3801 is a single width (4 TE) 6U (double euro form factor) card. It was designed with applications at neutron sources and synchrotrons in mind, but due to the units flexible design it (or other members of the family) can be used in many particle physics and related applications as well as in applied research. Possible applications include:

- Beam loss monitor readout
- Luminosity monitor readout
- Electron Microscope readout
- Polarimeter Applications
- Time resolved counter acquisition
- „Deadtimeless" scaler readout

This document was written with the focus on the user of the unit, who wants to integrate the board into a data acquisition system and interested parties who consider the module for future use in their setup and would like to get an overview on the designs capabilities.

The SIS360x/38xx card is a flexible concept to implement a variety of latch and counter firmware designs. The flexibility is based on two to six Xilinx FPGAs in conjunction with a FLASHPROM from which the firmware files are loaded into the FPGAs. Depending on the stuffing options of the printed circuit board, the user has the possibility to cover several purposes with the same card, hence the manual is a combination of firmware and hardware description .

This manual describes the firmware versions 5 and 6 of the SIS3801 multiscaler, which were developed for applications at the Advanced Photon Source (APS).

All cards of the family are equipped with the 5 row VME64x VME connectors, a side cover and EMC front panel, as well as the VIPA LED set. For users with VME64xP subracks VIPA extractor handles can be installed. The base board is prepared for VIPA style addressing, the current first version of the SIS3801 firmware does not feature VIPA modes yet however.

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm. A list of available firmware designs can be retrieved from http://www.struck.de/sis3638firm.htm

2   Technical Properties/Features

The SIS3801 is rather a firmware design in combination with given board stuffing options, than a name for the board (this is the reason, why the modules are named SIS360x/38xx on the front panel and the distinction of the units is made by the module identifier register). The firmware makes use of part of the possibilities of the SIS360x/38xx PCB, if the SIS3801 or other firmware designs of the family come close to what you need, but something is missing, a custom firmware design may be an option to consider.

Find below a list of key features of the SIS3801.
- 32 channels
- 200 MHz counting rate (ECL and NIM), 100 MHz for TTL
- 24/32-bit channel depth
- NIM/TTL/ECL versions
- flat cable (TTL/ECL) and LEMO (TTL/NIM) versions
- 64K FIFO (256 K available on request)
- A16/A24/A32 D16/D32/BLT32 (CBLT32 prepared)
- Base address settable via 5 rotary switches (A32-A12) and one jumper (A11)
- VME interrupt capability
- VIPA geographical addressing prepared
- VIPA LED set
- 3.8 µs minimum dwell time (with all channels active)
- 2 external user bits (in 24-bit mode)
- Reference Pulser capability
- Internal 10 MHz to LNE clock
- Prescaler for external and internal LNE signal
- Up to eight firmware files
- single supply (+5 V)

2.1   Board Layout

Xilinx FPGAs are the working horses of the SIS360x/38xx board series. The counter (prescaler, latch, ...) logic is implemented in one to four chips, each chip handles eight front end channels. The VME interface and the input and output control logic reside in two Xilinx chips also. The actual firmware is loaded into the FPGAs upon power up from a FLASHPROM under jumper control. The user can select among up to eight different boot files by the means of a 3-bit jumper array. The counter inputs, the control inputs and the outputs can be factory configured for ECL, NIM and TTL levels. The front panel is available as flat cable (ECL and TTL) or LEMO (NIM and TTL) version. The board layout is illustrated with the block diagram below:
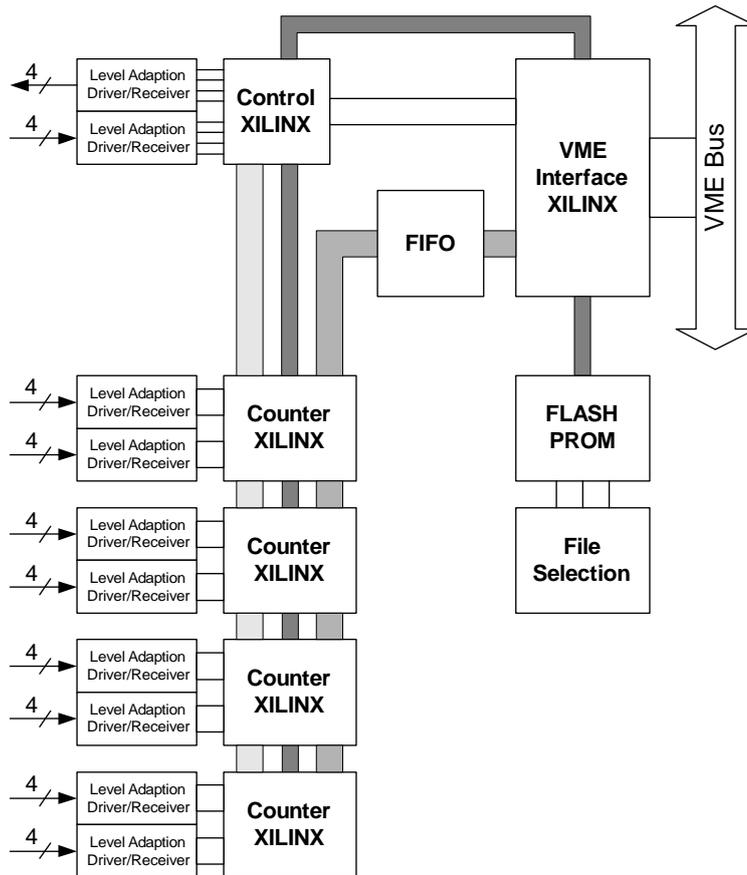
SIS3801 Block Diagram

2.2 Counter Design and Modus Operandi

The counters are implemented in XILINX FPGAs. One of the counter FPGAs holds 8 32-bit or 24-bit deep counter channels. Two counter banks are implemented, the actual multiscaling mechanism is implemented as bank switching between the two counter banks and copying the data of the inactive bank to the FIFO. Bank switching can be initiated via an external pulse or a VME command. A sketch of the bank mechanism can be found below.

In nuclear physics on refers to the time slice length (i.e. the period during which counts are acquired into the same bank) as dwell time. In many cases the dwell time will be constant, but the user is free to use varying time intervals, as long as the minimum time between two next event pulses is smaller than the minimum dwell time with the given number of active channels. An approach to measure the length of the time slices is the readout of a fixed frequency clock on one of the counter channels, the accuracy of the measurement is defined by the frequency stability of the clock and the interval length.

Firmware versions 5 and 6 are furnished with an internal 10 MHz pulser which can be routed via an LNE (Load Next Event) prescaler alternatively to the LNE front panel. This allows standalone readout with fixed time intervals as well as readout on the Nth occurrence of an external signal (like a clock tick from a shaft encoder or stepper motor).

LNE

CIP

8 Scaler Inputs	Bank 0
	Bank 1
	Counter Xilinx

to FIFO

LNE

CIP

8 Scaler Inputs	Bank 0
	Bank 1
	Counter Xilinx

to FIFO
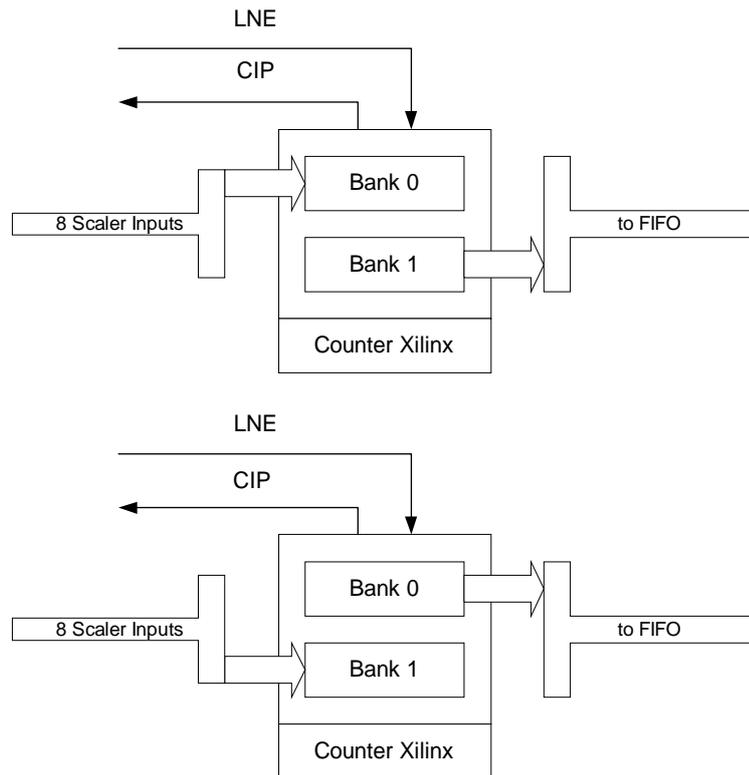
2.3 Minimum Dwell Time

The minimum dwell time on the SIS3801 isdefined by the time which is needed to copy the data from the idle scaler bank to the FIFO. The time required to copy one 32-bit data word from the counter Xilinx chips to the FIFO is 120 ns. The overhead is 260 ns, thus the minimum dwell time is some 4.0 μs with all 32 scaler channels active. The firmware designs 3,4,5 and 6 have a channel count dependent dwell time. Via the copy disable register the number of active channels can be reduced if lower dwell times are of interest. The time, which is needed for the copy progress can be measured on the copy in progress (CIP) output, the output is active for the duration of the process, the signal can also be of help to control or synchronise external components.

As the maximum number of counts the unit can acquire within microsecond time frames is in the order of a couple of hundred, one may consider to go for a 16-bit counter design if shorter dwell times are envisaged, the readout time is reduced to 50 ns/16-bit word in such a design (the FIFO is of 18-bit synchronous type).

2.4   Readout Considerations

One of the major advantages of a FIFO based counter/multiscaler is the decoupling of the time slice/bank switching and the actual VME readout of the data. Depending on the application the FIFO may be used to buffer one or two reads only, before a DSP processes the data on the fly, in this case the FIFO is used to establish readout pipelining, in other cases the maximum possible FIFO size is of interest to store a complete set of data points for a pulsed or non continuous measurement. Continuous multiscaling can be established as long as the VME master can cope with the amount of data generated by the scaler, i.e. the FIFO is never allowed to run into the FIFO full condition. The 64K default FIFO size of the SIS3801 V2 (4K on V1 boards) is considered to be a save value for most applications, for more demanding applications the FIFO size can be increased up to 256K as a stuffing option. One as to keep in mind, that two FIFO words are needed to hold one 32-bit scaler value, i.e. a 64K FIFO can hold 32K scaler words or 1K events (time slices) with all 32 channels enabled. The packing of the FIFO data into VME D32 words is handled without user intervention upon VME read cycles from the FIFO. In high data rate applications, the readout scheme will make use of the FIFO half full flag (or FIFO almost full flag in the 256K FIFO case) via a VME interrupt or polling in most cases, as a minimum known number of 32K (32K-64 respective) longwords can be read out (being blocked into smaller chunks by VME) with a block transfer.

Example: Assume 32 channels are read out with a dwell time of 10 μs (i.e. at a rate of 100 KHz) with a 64K FIFO unit. The data rate is 32 channels x 4 bytes x 100 KHz corresponding to some 12 MB/s. The FIFO half full interrupt or flag will be asserted for the first time after 0.5 ms of data acquisition, the VME master has to digest 64Kbytes within less than 0.5 ms (including IRQ handling or polling) to prevent the FIFO from overflow.

Note: No new data can be acquired before a FIFO reset if the FIFO full condition has occurred (i.e. the FIFO full condition is considered an error condition, which should not occur in standard operation).

2.5   Count Enable Logic

A channel acquires input or test counts, if the count enable and the global count enable conditions are true. Via the test enable toggle bits in the control register the input of the counter is switched to test pulses or front panel signals.
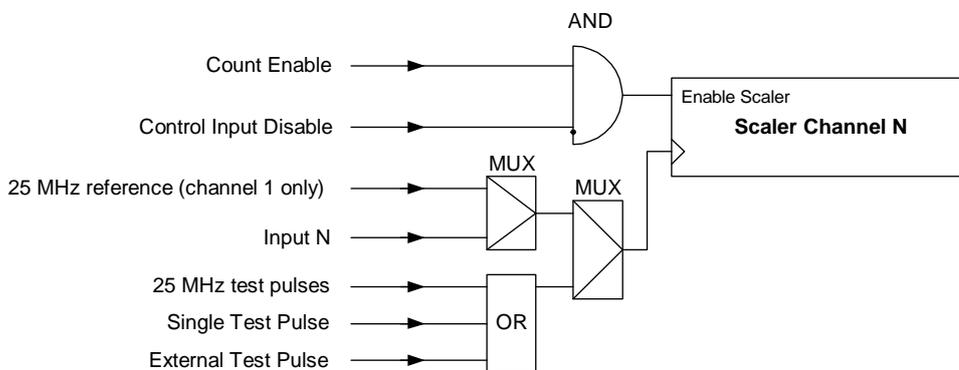
3 Getting Started

The minimum setup to operate the SIS3801 requires the following steps:

- Check the proper firmware design is selected (should be design zero, i.e. all jumpers of jumper array J500 set.
- Select the VME base address for the desired addressing mode
- Select the VME SYSRESET behaviour via J520
- turn the VME crate power off
- install the scaler in the VME crate
- connect your signals to the counter
- turn crate power back on
- issue a key reset by writing to 0x60
- issue FIFO clear by writing to 0x20
- enable next logic by writing to 0x28
- issue first next clock pulse to start counting by soft- or hardware
- after one or more subsequent next clock pulses data can be read from the FIFO from the addresses 0x100 through 0x1FC.

Note: Issuing a FIFO clear is essential on units with 256 K FIFO to synchronise the cascaded FIFO chips.

A good way of checking first time communication with the SIS3801 consists of switching on the user LED by a write to the control register at offset address 0x0 with data word 0x1 (the LED can be switched back off by writing 0x100 to the control register)..

3.1 Factory Default Settings

3.1.1 Adressing

SIS3801 boards are shipped with the EN_A32, the EN_A24 and the EN_A16 jumpers installed and the rotary switches set to:

Switch	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J A_11	Bits 7-4	Bits 3-0
Setting	3	8	3	8	3	8	0	0

Jumper A_11 is open (bit 11 set).
Hence the unit will respond to the following base addresses:

Mode	Base address
A32	0x38383800
A24	0x383800
A16	0x3800

Firmware Design
File 0 (SIS3801, Version 5) of the FLASHPROM is selected (all jumpers of jumper array J500 set).

3.1.2 System Reset Behaviour

J520 is set, i.e. the SIS3801 is reset upon VME reset.

4 Firmware Selection

The FLASH PROM of a SIS360x/38xx board can contain several boot files. A list of available FLASHPROM versions can be found on our web site http://www.struck.de in the manuals page. If your FLASHPROM has more than one firmware design, you can select the desired firmware via the firmware selection jumper array J500 . You have to make sure, that the input/output configuration and FIFO configuration of your board are in compliance with the requirements of the selected firmware design (a base board without FIFO can not be operated as multi channel scaler e.g.). A total of 8 boot files from the FLASHPROM can be selected via the three bits of the jumper array. The array is located towards the rear of the card between the VME P1 and P2 connectors. The lowest bit sits towards the bottom of the card, a closed jumper represents a zero, an open jumper a one.

4.1 Examples

The figures below show jumper array 500 with the soldering side of the board facing the user and the VME connectors pointing to the right hand side.
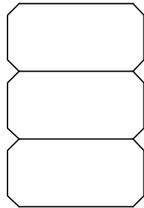
Bootfile 0 selected
With all jumpers closed boot file 0 is selected
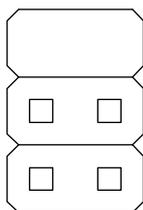
Bootfile 3 selected
With the lowest two jumpers open bit 0 and bit 1 are set to 1 and hence boot file 3 is selected

Front Panel LEDs

The SIS3801 has 8 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs (VME user LED, Clear, Copy in Progress, Scaler enable and VIPA user LED).

Designation	LED	Color	Function
A	Access	yellow	Signals VME access to the unit
P	Power	red	Flags presence of VME power
R	Ready	green	Signals configured logic
U	VME user LED	green	To be switched on/off under user program control
CLR	Clear	yellow	Signals bank clear
OVL (CIP)	Copy in Progress	red	Signals copy in progress
S	Scaler Enable	green	Signals one or more enabled channels
VU	VIPA user LED	green	for future use

The LED locations are shown in the portion of the front panel drawing below.
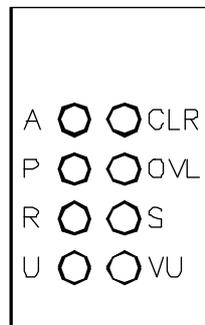
The VME Access, the Clear and the Scaler enable LED are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to the chapter 16.1).

5   VME addressing

5.1   Address Space

As bit 11 is the lowest settable bit on the 360x/38xx board, an address space of 2 Kbytes (Offset plus 0x000 to 0x7ff) is occupied by the module.

5.2   Base Address

5.2.1   VME

The VME addressing mode (A16/A24/A32) is selected via the jumpers EN_A16, EN_A24 and EN_A32.The mode is selected by closing the corresponding jumper, it is possible to enable two or all three addressing modes simultaneously.

The base address is set via the five rotary switches SW_A32U, SW_A32L, SW_A24U, SW_A24L and SW_A16 and the jumper J_A11. The table below lists the switches and jumpers and their corresponding address bits.

Switch/Jumper	Affected Bits
SW_A32U	31-28
SW_A32L	27-24
SW_A24U	23-20
SW_A24L	19-16
SW_A16	15-12
J_A11	11

In the table below you can see, which jumpers and switches are used for address decoding in the three different addressing modes (fields marked with an x are used).

	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J_A11
A32	x	x	x	x	x	x
A24			x	x	x	x
A16					x	x

Note: J_A11 closed represents a 0, J_A11 open a one

5.2.2   VIPA/VME64x

As the VME64x and the VME64xP (VIPA) standard are not yet standards to refer to and to declare conformity with, addressing modes (like geographical addressing e.g.) according to these standards are prepared but not yet implemented in the current firmware revisions.

5.3   Address Map

The SIS360x/38xx boards are operated via VME registers, VME key addresses and the FIFO (where installed). The following table gives an overview on all SIS3801 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.

Offset	Key	Access	Type	Function
0x000		R/W	D16/D32	Control and Status register
0x004		R/W	D16/D32	Module Identification and IRQ control register
0x008		R	D16/D32	Acquisition count register
0x008		W	D16/D32	Acquisition preset register
0x00C		W	D16/D32	Copy disable register
0x010		W	D16/D32	Write to FIFO (in FIFO test mode)
0x020	KA	W	D16/D32	clear FIFO, logic and counters
0x024	KA	W	D16/D32	VME next clock
0x028	KA	W	D16/D32	Enable next clock logic
0x02C	KA	W	D16/D32	Disable next clock logic
0x050	KA	W	D16/D32	enable reference pulser channel 1
0x054	KA	W	D16/D32	disable reference pulser channel 1
0x058	KA	W	D16/D32	set ROAK style interrupter/disable RORA (Firmware Versions 0xB and 0xC only)
0x05C	KA	W	D16/D32	set RORA style interrupter/disable ROAK (Firmware Versions 0xB and 0xC only)
0x060	KA	W	D16/D32	reset register (global reset)
0x068	KA	W	D16/D32	Test pulse (generate a single pulse)
0x080		R/W	D16/D32	Prescaler factor register
0x100-0x1FC		R/(W)	D32/BLT32	read FIFO

Note: D08 is not supported by the SIS38xx boards

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

6   Register Description

6.1   Status Register (0x0)

The status register reflects the current settings of most of the SIS3801 parameters in read access, in write access it functions as the control register.

Bit	Function
31	Status VME IRQ source 3 (FIFOalmost full)
30	Status VME IRQ source 2 (FIFO half full)
29	Status VME IRQ source 1 (FIFO full)
28	Status VME IRQ source 0 (start of CIP)
27	VME IRQ
26	internal VME IRQ
25	Status interrupter style (0=RORA, 1=ROAK)
24	0
23	Status VME IRQ Enable Bit Source 3
22	Status VME IRQ Enable Bit Source 2
21	Status VME IRQ Enable Bit Source 1
20	Status VME IRQ Enable Bit Source 0
19	software disable counting bit (0=count enable, 1=count disable)
18	Status external disable
17	Status enable external clear
16	Status enable external next
15	Status Enable next logic
14	0
13	Status enable reference pulser channel 1
12	FIFO flag full
11	FIFO flag almost full0 (inverted almost empty flag on 256K units with V3 FIFO GAL)
10	FIFO flag half full
9	FIFO flag almost empty (inverted on 256K units)
8	FIFO flag empty
7	Status enable LNE prescaler
6	Status 10 MHz to LNE prescaler
5	Status input test mode
4	Status 25 MHz test pulses
3	Status input mode bit 1
2	Status input mode bit 0
1	Status FIFO test mode
0	Status user LED

The reading of the status register after power up or key reset is 0x300 with 64K FIFO installed and 0x100 with 256 K FIFO installed (see default settings of control register).

6.2   Control Register (0x0)

The control register is in charge of the control of most of the basic properties of the SIS3801 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.

On read access the same register represents the status register.

Bit	Function
31	disable IRQ source 3 (*)
30	disable IRQ source 2 (*)
29	disable IRQ source 1 (*)
28	disable IRQ source 0 (*)
27	clear software disable counting bit (*)
26	disable external disable (*)
25	disable external clear (*)
24	disable external next (*)
23	enable IRQ source 3
22	enable IRQ source 2
21	enable IRQ source 1
20	enable IRQ source 0
19	set software disable counting bit
18	enable external disable
17	enable external clear /enable external LNE (**)
16	enable external next
15	disable LNE prescaler (*)
14	disable 10 MHz to LNE prescaler (*)
13	disable input test mode (*)
12	disable 25 MHz test pulses (*)
11	clear input mode bit 1 (*)
10	clear input mode bit 0 (*)
9	disable FIFO test mode
8	switch off user LED (*)
7	enable LNE prescaler
6	enable 10 MHz to LNE prescaler
5	enable input test mode
4	enable 25 MHz test pulses
3	set input mode bit 1
2	set input mode bit 0
1	enable FIFO test mode
0	switch on user LED

(*) denotes the default power up or key reset state
(**)"enable external LNE" versions V7, V8, V9, VA only

6.3   Module Identification and IRQ control register (0x4)

This register has two basic functions. The first is to give information on the active firmware design. This function is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3801 or 3600 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3801 for example has the 24-bit mode with user bits and the straight 32-bit mode as versions.

Bit	Read/Write access	Function	
31	read only	Module Identification Bit 15	Module Id Digit 3
30	read only	Module Identification Bit 14	
29	read only	Module Identification Bit 13	
28	read only	Module Identification Bit 12	
27	Read only	Module Identification Bit 11	Module Id Digit 2
26	read only	Module Identification Bit 10	
25	read only	Module Identification Bit 9	
24	read only	Module Identification Bit 8	
23	read only	Module Identification Bit 7	Module Id Digit 1
22	read only	Module Identification Bit 6	
21	read only	Module Identification Bit 5	
20	read only	Module Identification Bit 4	
19	read only	Module Identification Bit 3	Module Id Digit 0
18	read only	Module Identification Bit 2	
17	read only	Module Identification Bit 1	
16	read only	Module Identification Bit 0	
15	read only	Version Bit 3	
14	read only	Version Bit 2	
13	read only	Version Bit 1	
12	read only	Version Bit 0	
11	read/write	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	
10	read/write	VME IRQ Level Bit 2	
9	read/write	VME IRQ Level Bit 1	
8	read/write	VME IRQ Level Bit 0	
7	read/write	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle (*)	
6	read/write	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle (*)	
5	read/write	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle (*)	
4	read/write	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle (*)	
3	read/write	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle (*)	
2	read/write	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle (*)	
1	read/write	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	
0	read/write	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	

(*): Version VD and VE are bits 7 to 2 not programmable. Are set to 0.

The second function of the register is interrupt control. The interrupter type of the SIS3801 is D08(O) . Via bits 0-7 of the module identifier and interrupt control register you can define the interrupt vector, which is placed on the VME bus during the interrupt acknowledge cycle. Bits 8 through 10 define the VME interrupt level, bit 11 is used to enable (bit set to 1) or disable (bit set to 0) interrupting.

Module identification and version example:
The register for a SIS3801 in straight 32-bit mode (version 1) reads 0x38011nnn, for a SIS3801 in 24-bit mode (version 2) it reads 0x38012nnn. (the status of the lower 3 nibbles is denoted with n in the example).

6.4   Acquisition count register 0x8

This 32-bit wide read only register holds the number of acquisitions (**19** bits). It is cleared with the start operation and incremented with consecutive LNE pulses. The contents of the acquisition count register is compared with the contents of the acquisition preset register. Acquisition is completed as soon as the acquisition count is equal than the acquisition preset value and if the mode is enabled.

Bit	Function
31	0
...	...
19	0
18	bit 18 of acquisition count
...	...
0	bit 0 of acquisition count

6.5   Acquisition preset register 0x8

This write only register allows you to define the number of counting periods to acquire. The preset value is **18**-bit wide. A preset value of N results in stopping operation after N+1 LNEs if Acquisition Preset Stop mode is enabled (bit 31=1).
Further LNEs are ignored after completion of acquisition until a key reset acquisition VME access is performed.

Bit	Function
31	Enable Acquisition Preset Stop mode
30	no
...	...
18	no
17	bit 17 of preset value
...	...
0	bit 0 of preset value

6.6   Copy disable register 0xC

The copy disable register implementation of firmware versions 5 and 6 is derived from version 3 and, i.e. the dwell time depends on the number of active channels. In these firmware implementations the first set bit (counting from zero) will define the end of the copy process loop and the duration of the copy in progress and hence the minimum dwell time depends on the number of enabled channels.

Version V5 to VC:
Due to space limitations in the control Xilinx chip bits 31 through **25** can not be set (i.e. have the same status as bit **24**). Hence you can operate the multiscaler with **1 to 24** or all 32 channels enabled.

Version VD and VE:
Due to space limitations in the control Xilinx chip bits 31 through **17** can not be set (i.e. have the same status as bit 1**6**). Hence you can operate the multiscaler with **1 to 16** or all 32 channels enabled.

The copy time was measured to be some 120 ns/channel, an overall overhead in the order of 260 ns. This allows you to make measurements with very short dwell times with a limited number of channels.
Example: If 0x10 is written to the copy disable register, the data of channels 1 through 4 are copied into the FIFO, all other channels are disabled. The minimum dwell time is in the order of 750 ns (4 channels x 120 ns+260 ns overhead, the exact value can be measured on the CIP output) for this example.

6.7   LNE prescale factor register 0x80

6.7.1 V7 and V8

The LNE prescale factor register allows you to either prescale the front panel LNE pulse (clock ticks from an angular encoder e.g.) or the internal 10 MHz to prescaler clock, if the pulser is enabled. The prescale factor is a 24-bit (28-bit in V9 and VA) value. The second case allows you to run the multiscaler with a fixed time slice length. The register can be reprogrammed while the scaler acquires data as long as the user makes sure not to change the prescale factor while an internal reload is in progress. The period between two CIP pulses is safe for reprogramming. Programming the prescale factor to 0 results in routing the raw signal to the LNE. If the LNE rate after the prescaler is higher than the possible maximum, excess LNE pulses are ignored, the CIP output allows you to monitor the accepted LNE pulses.
If the new prescale factor is supposed to have an immediate effect (i.e. if the new prescale factor and the input rate are smaller than the previous setting), following sequence has to be used:

1.) disable LNE prescaler (write 0x8000 to control register)
2.) set new prescale factor
3.) enable LNE prescaler (write 0x80 to control register)

The LNE prescale factor is given by **register value+1.**
If the an output mode with CIP front panel output is enabled, the CIP signal can be used to synchronise external hardware to the actual LNE pulses after prescaling.

Example: If 9999 (decimal) is written to the LNE prescale factor register with the prescaler and the 10 MHz to prescaler enabled (via bits 6 and 7 of the control register), the scaler will get LNE pulses with a frequency of 1 KHz.

Note: Software LNE pulses are not routed to the LNE prescaler, they do always initiate a bank switch/time slice advance.

6.7.2 V9 and VA

The prescale factor was extended to 28-bits in version 9 and A of the SIS3801.

6.8 FIFO (0x100-0x1FC)

The FIFO can be accessed from addresses 0x100 through 0x1FC to facilitate the readout with different types of CPUs. For masters with block transfer capability without address increment its most convenient to read all data from address 0x100. For masters with block transfer address auto increment it is straightforward to set up repeated block reads with a length of 256 Bytes (the maximum VME block transfer size) from address 0x100 (and the autoincrement uses the addresses 0x100 through 0x1FC for the transfer).

If FIFO test mode is enabled data can be written to the FIFOs addresses.

7 Broadcast Addressing

Broadcast addressing options, which are part of SIS3801 firmware versions 1-4 are not available in firmware version 5 and 6 due to restrictions of the Xilinx control chip.

8   VME Interrupts

Four VME interrupt sources are implemented in the SIS3801 firmware design:

- start of CIP
- FIFO half full
- FIFO almost full
- FIFO full (error condition)

The interrupter is of type D8(O).

If the unit is equipped with four FIFO chips, the FIFO half full flag can not be used to generate a useful interrupt condition. In this case the FIFO almost full flag is set upon the FIFO almost empty condition being cleared, i.e. at 25-50% filling level, what gives the user reasonable safety regarding the readout time..

The interrupt logic is shown below. For VME interrupt generation the corresponding interrupt source has to be enabled by setting the respective bit in the VME control register (disabling is done with the sources J/K bit). Interrupt generation has to be enabled by setting bit 11 in the IRQ and version register. The internal VME interrupt flag can be used to check on an IRQ condition without actually making use of interrupts on the bus.

The VME interrupt level (1-7) is defined by bits 8 through 10, and the VME interrupt vector (0-255) by bits 0 through 7 of the VME IRQ and version register.

In general an interrupt condition is cleared by disabling the corresponding interrupt, clearing the interrupt condition (i.e. clear overflow) and enabling the IRQ again.

Note: In most cases your experiment may not require interrupt driven scaler readout, but the interrupt capability of the SIS3801 provides a way to overcome the problem of missing front panel inputs on most commercial VME CPUs.
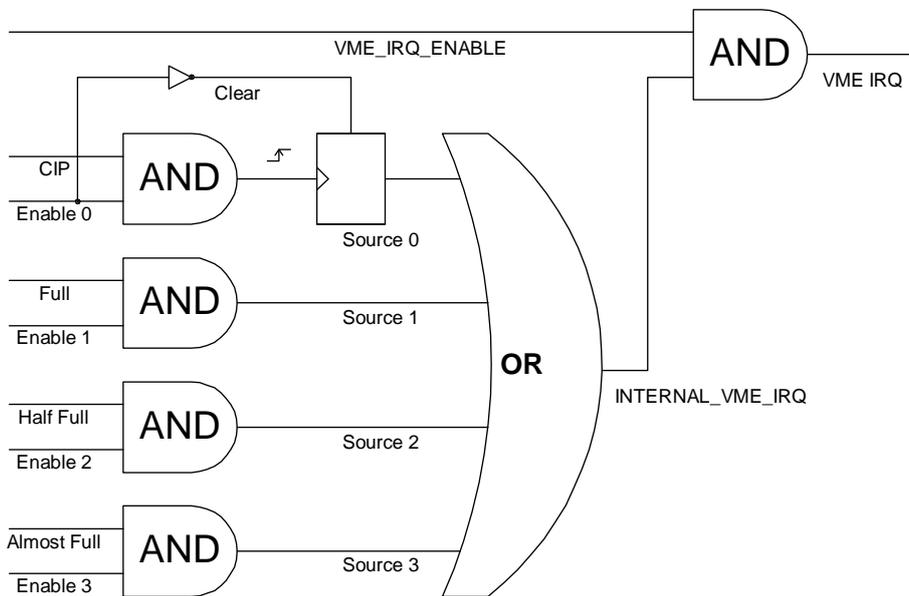
9   Data Format

The data format of the actual counter values is described for the two operating modes (24/32-bit) and the two possible data word widths (D16/D32) in this section.

9.1   32-bit Mode (Version 1,3 and 5)

In these modes the data word contains the straight scaler contents.

9.1.1 D16

	high Byte	low Byte
first read	Data Bits 31-24	Data Bits 23-16
second read	Data Bits 15-8	Data Bits 7-0

9.1.2 D32

Data Bits 31-24	Data Bits 23-16	Data Bits 15-8	Data Bits 7-0

9.2   24-bit Mode (Version 2,4 and 6)

In these modes the lower 24 bits hold the scaler value, the upper eight data bits contain the latched status of the two user bits and the bank and channel information. The bit names and their function are listed in the table below.

Bit	Contents
U1	User Bit 1
U0	User Bit 0
B	Bank number (0/1)
C4	Channel number Bit 4
C3	Channel number Bit 3
C2	Channel number Bit 2
C1	Channel number Bit 1
C0	Channel number Bit 0

9.2.1 D16

	high Byte								low Byte
first read	U1	U0	B	C4	C3	C2	C1	C0	Data Bits 23-16
second read	Data Bits 15-8								Data Bits 7-0

9.2.2 D32

| U1	U0	B	C4	C3	C2	C1	C0	Data Bits 23-16	Data Bits 15-8	Data Bits 7-0

10 Input Configuration

SIS36/38xx boards are available for NIM, TTL and ECL input levels and in LEMO and flat cable versions. The boards are factory configured for the specified input level and connector type, input termination is installed.

10.1 ECL

The 100 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

| Network	Channels	1 K Networks
RN10	1-4	RN11/12
RN20	5-8	RN21/22
RN30	9-12	RN31/32
RN40	13-16	RN41/41
RN50	17-20	RN51/52
RN60	21-24	RN61/62
RN70	25-28	RN71/72
RN80	29-32	RN81/82
RN110	Control 1-4	RN111/RN112
RN120	Control 5-8	RN121/RN122

The schematics of the ECL input circuitry is shown below.
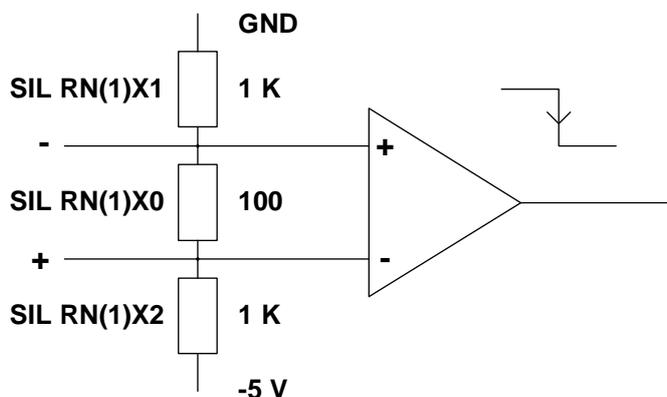
10.2 NIM

The 50 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels
U15 (Pins 10 to 6)	1-4
U15 (Pins 1 to 5)	5-8
U35 (Pins 10 to 6)	9-12
U35(Pins 1 to 5)	13-16
U55 (Pins 10 to 6)	17-20
U55 (Pins 1 to 5)	21-24
U75 (Pins 10 to 6)	25-28
U75 (Pins 1 to 5)	29-32
U115 (Pins 10 to 6)	Control 1-4
U115 (Pins 1 to 5)	Control 5-8

The schematics of the NIM input circuitry is shown below.
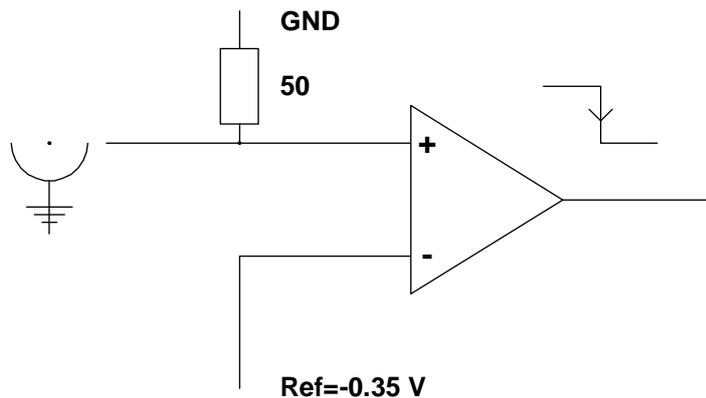
10.3 TTL

The TTL input level option is possible with LEMO and flat cable connectors.

10.3.1 TTL/LEMO

The (low active) TTL/LEMO input circuitry is sketched below. A high active version can be implemented by replacing the 74F245 with a 74F640

5 V

1 K

245
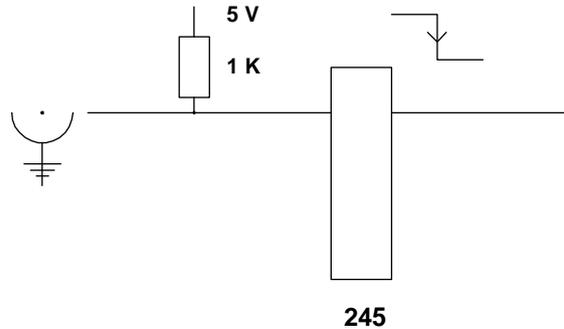
10.3.2 TTL/Flat Cable

In the flat cable TTL version the positive (right hand side) of the connector is tied to ground.

5 V

1 K

-

+

245
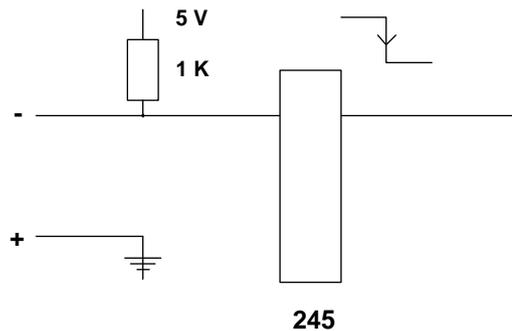
11 TTL output configuration

Standard TTL units drive high impedance signals (i.e. 24 mA current), a 50 Ω driver piggy (driving 48 mA) pack is available on request. It plugs into the socket U170 instead of the standard driver chip.

12 Connector Specification

The four different types of front panel and VME connectors used on the SIS360x and SIS38xx boards are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
20 pin header	Control (flat cable versions)	DIN41651 20 Pin (AMP e.g.)
34 pin header	Inputs (flat cable versions)	DIN41651 34 Pin (AMP e.g.)
LEMO	Control and Input (LEMO versions)	LEMO ERN.00.250.CTL

13 Control Input Modes

The assignment of the control inputs can be controlled via the input mode bits in the control register. While the standard SIS3800 firmware design (design 3800 version 1) has inputs only, design 3800 version 2 is compatible with boards, where control lines 5 to 8 are configured as outputs (what is the case for SIS3801 multiscaler boards).

13.1 Inputs

Control Input Modes	V1-V6	V7, V8, V9 and VA
Mode 0 (bit1=0, bit0=0):	input 1 -> external next pulse	input 1 -> external next pulse
	input 2 -> external user bit 1	input 2 -> external user bit 1
	input 3 -> external user bit 2	input 3 -> external user bit 2
	input 4 -> reset	input 4 -> inhibit LNE
Mode 1 (bit1=0, bit0=1):	input 1 -> external next pulse	input 1 -> external next pulse
	input 2 -> external user bit 1	input 2 -> external user bit 1
	input 3 -> disable counting	input 3 -> disable counting
	input 4 -> reset	input 4 -> inhibit LNE
Mode 2 (bit1=1, bit0=0):	input 1 -> external next pulse	input 1 -> external next pulse
	input 2 -> external user bit 1	input 2 -> external user bit 1
	input 3 -> external user bit 2	input 3 -> external user bit 2
	input 4 -> disable counting	input 4 -> disable counting
Mode 3 (bit1=1, bit0=1):	input 4 -> external test	input 4 -> external test

13.2 Outputs

Four ouput signals are defined on the SIS3801 board. They are copy in progress (CIP), FIFO empty, FIFO half full and FIFO full (ERROR). Their assignments to the control lines are listed in the table below.

Signal	Control Signal
CIP	5
FIFO empty	6
FIFO half full	7
FIFO full	8

14 Signal Specification

14.1 Control Signals

The width of the clear and external next pulse has to be greater or equal 10 ns, an external inhibit (disable counting) has to be present for the period you desire to disable counting. An internal delay of some 15 ns has to be taken into account for all external signals.

14.2 Inputs

The SIS3801 is specified for counting rates of 200 MHz for ECL and NIM signals and 100 MHz for the TTL case. Thus the minimum high and low level duration is 2.5 ns (5 ns respective). Signal deterioration over long cables has to be taken into account.

14.3 User Bits

The status of the user bits (Version 2,4 and 6) is latched with the leading edge of the external next pulse. A setup time of greater equal 10 ns and a hold time of 25 ns is required, i.e. the signal should have a length of greater 35 ns and has to be valid 10 ns before the leading edge of the next clock pulse arrives.

15 Operating conditions

15.1 Power Consumption/Voltage requirement

Although the SIS3801 is prepared for a number of VIPA features, it was decided to use an ob board DC/DC converter to generate the –5 V, which are needed for driver and receiver chips, to allow for the use of the module in all 6U VME environments. The power consumption is counting rate dependent, it varies from the idle value of +5 V 3,3 A to +5 V 4,5 A with all channels counting at 200 MHz(i.e. the power consumption is < 23 W).

15.2 Cooling

Forced air flow is required for the operation of the SIS3801 board.

15.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3801 scalers.
The leading pins on the SIS3801 VME64x VME connectors and connected on board circuitry are designed for hot swap in conjunction with a VME64x backplane (a VME64x backplane can be recognised by the 5 row VME connectors, while the standard VME backplane has three row connectors only).

16 Test

The SIS380x scaler series provides the user with a number of test features, which allow for debugging of the unit as well as for overall system setups.

16.1 LED (selftest)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic.

16.2 Internal pulser tests

16.2.1 Single Pulse

A single pulse into all channels can be generated with a write to the key address 0x68 if test mode is enabled via the control register. In conjunction with the count enable register more complex count patterns, like increment patterns e.g., can be generated before readout.

16.2.2 25 MHz Pulser

Simultaneous pulsing at 25 MHz into all channels can be used to test the complete readout chain and internal counter logic of the SIS3801. The feature is activated by enabling input test mode and 25 MHz test pulses via the corresponding bits in the control register.
The 25 MHz test pulser gives easy access to your VME CPUs readout timing. By making subsequent reads to the same counter and multiplying the difference in counts with 40 ns you can measure the single word access time.

16.3 Reference pulser channel 1

The reference pulser for channel 1 can be seen rather as a monitoring feature than a test feature. It sets the counting rate of channel 1 to 25 MHz (note, that a simultaneous front panel signal on channel 1 is ignored).

16.4 Signal-Input Priority

If the user happens to enable more than one input option (enable test mode, enable reference pulser, scaler enable) at the same time, the priority is as show in the table below:

Priority	Feature
1	Test mode
2	Reference Pulser (channel 1 only)
3	Front Panel Inputs

Example: If test mode and reference pulser are enabled at the same time, channel one will count test pulses (i.e. will count synchronous with the test pulser).

16.5 LNE source-Priority

A software LNE pulse is always passed to the logic. If the user happens to enable the internal 10 MHz pulser and the front panel LNE signal at the same time the actual used LNE source depends on the status of the prescaler enable.

If the LNE prescaler is enabled and both the internal and external LNE sources are disabled, the channel 1 input signal will be used as LNE source. Channel 1 will not count external pulses in this case, but can be used to count pulses from the 25 MHz reference pulser.
Find below a summary of the possible combinations:

External	Internal	Prescaler	LNE Source
0	0	0	soft only
0	0	1	channel 1
0	1	0	soft only
0	1	1	int. prescaled
1	0	0	ext
1	0	1	ext prescaled
1	1	0	ext
1	1	1	int. prescaled

16.6 FIFO Test

FIFO tests via the VME bus are helpful to debug the FIFO on the SIS38xx in case of spurious data and to debug an overall VME system with driver problems on the CPU side or flaky VME termination e.g.. In FIFO test mode the user can write defined data into the units FIFO via the VME bus and to compare them wit the read back result.
FIFO test mode is enabled by setting bit one of the control register and disabled by setting bit 9 of the control register. With FIFO test mode enabled data can be written to the FIFO at the address offset +0x100 (through 0x1FC). Writing to the location with FIFO mode

17 Software Support

VME multiscaler boards are tested at SIS with an OR VP6 VME CPU (Pentium II based) under Windows 95 and a National Instruments CVI user interface. The actual VME C code makes use of the OR Windows 95 DLL, which has straightforward to read and understand routines like:

```
VMEA24StdWriteWord(a32address + KEY_RESET, 0x0);    /* Key Reset */
rdata = VMEA24StdReadWord(a32address + STAT_REG);
```

In most cases the user setup will be using different hardware, a full fleshed real time operating system like VxWorks, and a different user interface. We still believe, that it is helpful to have a look at the code which is used to test the units and to take it as an example for the implementation of the actual scaler readout application. A floppy with our test software is enclosed with SIS3801 shipments.

Depending on the user feedback and co-operation we expect, that we will have drivers or at least example routines for the commonly used VME CPU operating systems at hand in the mid term.

17.1 Contents of the included Floppy

The Floppy contains a readme.txt file with the most up to date information, the CVI project file and all home made files from the project. The important part of the code for the implementation of your own program is sitting in the CVI call back routines.

18 Appendix

18.1 Address Modifier Overview

Find below the table of address modifiers, which can be used with the SIS360x/38xx (with the corresponding addressing mode enabled).

AM code	Mode
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3B	A24 non-privileged block transfer (BLT)
0x39	A24 non-privileged data access
0x2D	A16 supervisory access
0x29	A16 non-privileged access
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0B	A32 non-privileged block transfer (BLT)
0x09	A32 non privileged data access
	Future option: CBLT

18.2 Front Panel Layout

The front panel of the SIS3801 is equipped with 8 LEDs, 8 control in- and outputs and 32 counter inputs. On flat cable units (ECL and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the counter inputs are grouped into 2 blocks of 16 channels. A mixed LMEO control/flat cable counter input version is available also. The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VIPA crate at a later point in time.

In the drawing below you can find the flat cable (left hand side), the LEMO control/flat cable input (middle) and Lemo front panel layouts.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown
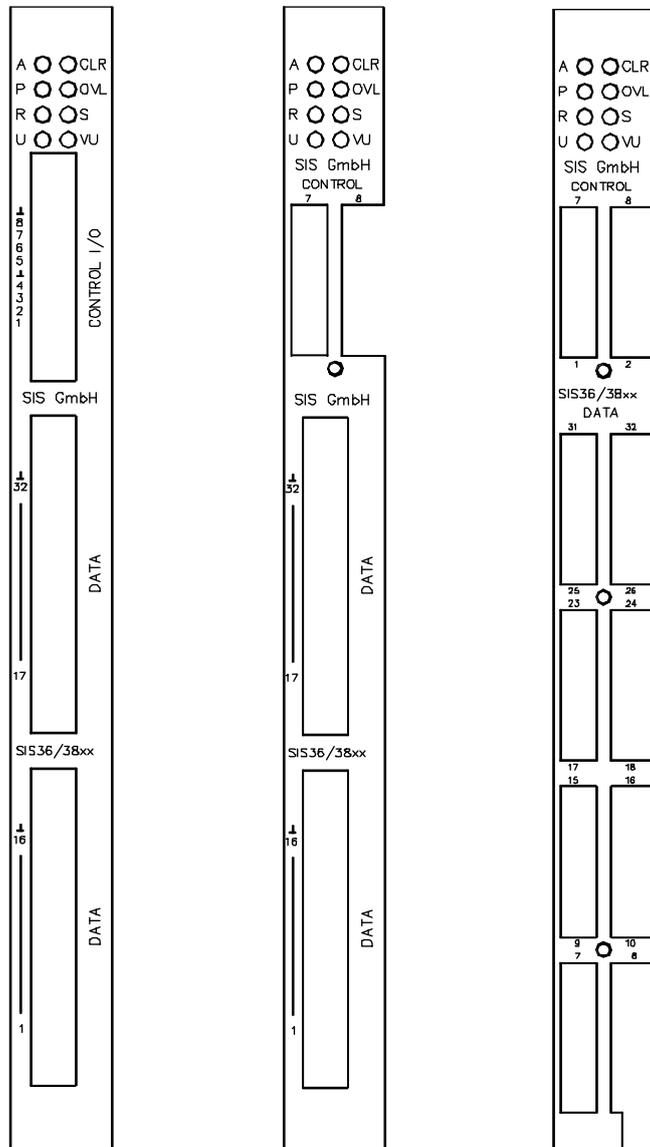
18.3 Flat cable Input/Output Pin Assignments

18.3.1 ECL

Data-Connector Channel 1-16   Data-Connector Channel 17-32

PIN	SIGNAL	SIGNAL	PIN
32	IN16 -	IN16 +	31
30	IN15 -	IN15 +	29
28	IN14 -	IN14+	27
26	IN13 -	IN13 +	25
24	IN12 -	IN12 +	23
22	IN11 -	IN11 +	21
20	IN10 -	IN10 +	19
18	IN9 -	IN9 +	17
16	IN8 -	IN8 +	15
14	IN7 -	IN7 +	13
12	IN6 -	IN6 +	11
10	IN5 -	IN5 +	9
8	IN4 -	IN4 +	7
6	IN3 -	IN3 +	5
4	IN2 -	IN2 +	3
2	IN1 -	IN1 +	1

PIN	SIGNAL	SIGNAL	PIN
32	IN32 -	IN32 +	31
30	IN31 -	IN31 +	29
28	IN30 -	IN30 +	27
26	IN29 -	IN29 +	25
24	IN28 -	IN28 +	23
22	IN27 -	IN27 +	21
20	IN26 -	IN26 +	19
18	IN25 -	IN25 +	17
16	IN24 -	IN24 +	15
14	IN23 -	IN23 +	13
12	IN22 -	IN22 +	11
10	IN21 -	IN21 +	9
8	IN20 -	IN20 +	7
6	IN19 -	IN19 +	5
4	IN18 -	IN18 +	3
2	IN17 -	IN17 +	1

Front view   Front view

INx + = ECL High active   INx + = ECL High active
INx - = ECL Low active   INx - = ECL Low active

Control-Connector Input 1-4 /Output 5-8

PIN	SIGNAL	SIGNAL	PIN
20	GND	GND	19
18	OUT8-	OUT8+	17
16	OUT7-	OUT7+	15
14	OUT6-	OUT6+	13
12	OUT5-	OUT5+	11
10	GND	GND	9
8	IN4 -	IN4 +	7
6	IN3 -	IN3 +	5
4	IN2 -	IN2 +	3
2	IN1 -	IN1 +	1

Front view

INx + = ECL High active
INx - = ECL Low active

OUTx + = ECL High active
OUTx - = ECL Low active

18.3.2 TTL

Data-Connector Channel 1-16

PIN	SIGNAL	SIGNAL	PIN
32	IN16 -	GND	31
30	IN15 -	GND	29
28	IN14 -	GND	27
26	IN13 -	GND	25
24	IN12 -	GND	23
22	IN11 -	GND	21
20	IN10 -	GND	19
18	IN9 -	GND	17
16	IN8 -	GND	15
14	IN7 -	GND	13
12	IN6 -	GND	11
10	IN5 -	GND	9
8	IN4 -	GND	7
6	IN3 -	GND	5
4	IN2 -	GND	3
2	IN1 -	GND	1

Front view

INx - = TTL Low active (74F245)

Data-Connector Channel 17-32

PIN	SIGNAL	SIGNAL	PIN
32	IN32 -	GND	31
30	IN31 -	GND	29
28	IN30 -	GND	27
26	IN29 -	GND	25
24	IN28 -	GND	23
22	IN27 -	GND	21
20	IN26 -	GND	19
18	IN25 -	GND	17
16	IN24 -	GND	15
14	IN23 -	GND	13
12	IN22 -	GND	11
10	IN21 -	GND	9
8	IN20 -	GND	7
6	IN19 -	GND	5
4	IN18 -	GND	3
2	IN17 -	GND	1

Front view

INx - = TTL Low active (74F245)

Control-Connector Input 1-4 /Output 5-8

PIN	SIGNAL	SIGNAL	PIN
20	GND	GND	19
18	OUT8-	GND	17
16	OUT7-	GND	15
14	OUT6-	GND	13
12	OUT5-	GND	11
10	GND	GND	9
8	IN4 -	GND	7
6	IN3 -	GND	5
4	IN2 -	GND	3
2	IN1 -	GND	1

Front view

INx - = TTL Low active (74F245)

OUTx - = TTL Low active (74F244)

18.4 List of Jumpers

Find below a list of the jumpers and jumper arrays.

Jumper Name	Array/Single	Function
J101	Single	Input Termination Control Input 1
J102	Single	Input Termination Control Input 2
J103	Single	Input Termination Control Input 3
J104	Single	Input Termination Control Input 4
J105	Single	Input Termination Control Input 5
J106	Single	Input Termination Control Input 6
J107	Single	Input Termination Control Input 7
J108	Single	Input Termination Control Input 8
J115	Single	Level Configuration (not for end user)
J500	Array	Boot File Selection
J520	Single	VME SYSRESET Behaviour
EN_A16	Single	Enable A16 addressing
EN_A24	Single	Enable A24 addressing
EN_A32	Single	Enable A32 addressing
J_A11	Single	Address Bit 11 Selection

18.5 Jumper and rotary switch locations

18.5.1 Addressing mode and base address selection

The EN_A32, EN_A24, EN_A16, A_11 and the 5 rotary switches are located int the middle of the upper section of the board close to the DC/DC converter, the corresponding section of the PCB is shown below.
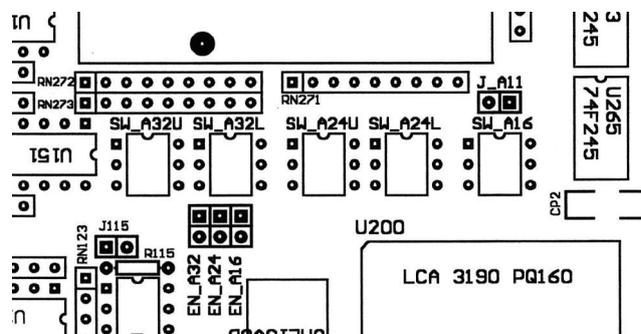
18.5.2 J500 (Bootfile Selection) and J520 (SYSRESET Behaviour)

The jumper array J500 is located between the P1 and the P2 connector. An open position in J500 defines a one (see also chapter 3), the lowest bit is next to the P2 connector.. J520 is located to the left of J500 and closer to the DC-DC converter. With jumper J520 closed the SIS3801 executes a key reset upon the VME SYSRESET signal. The section of the board with the jumper array and the SYSRESET jumper is shown below.
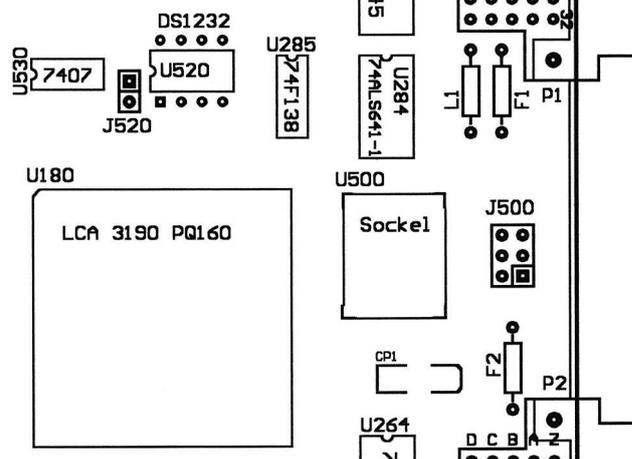
18.6 Board Layout
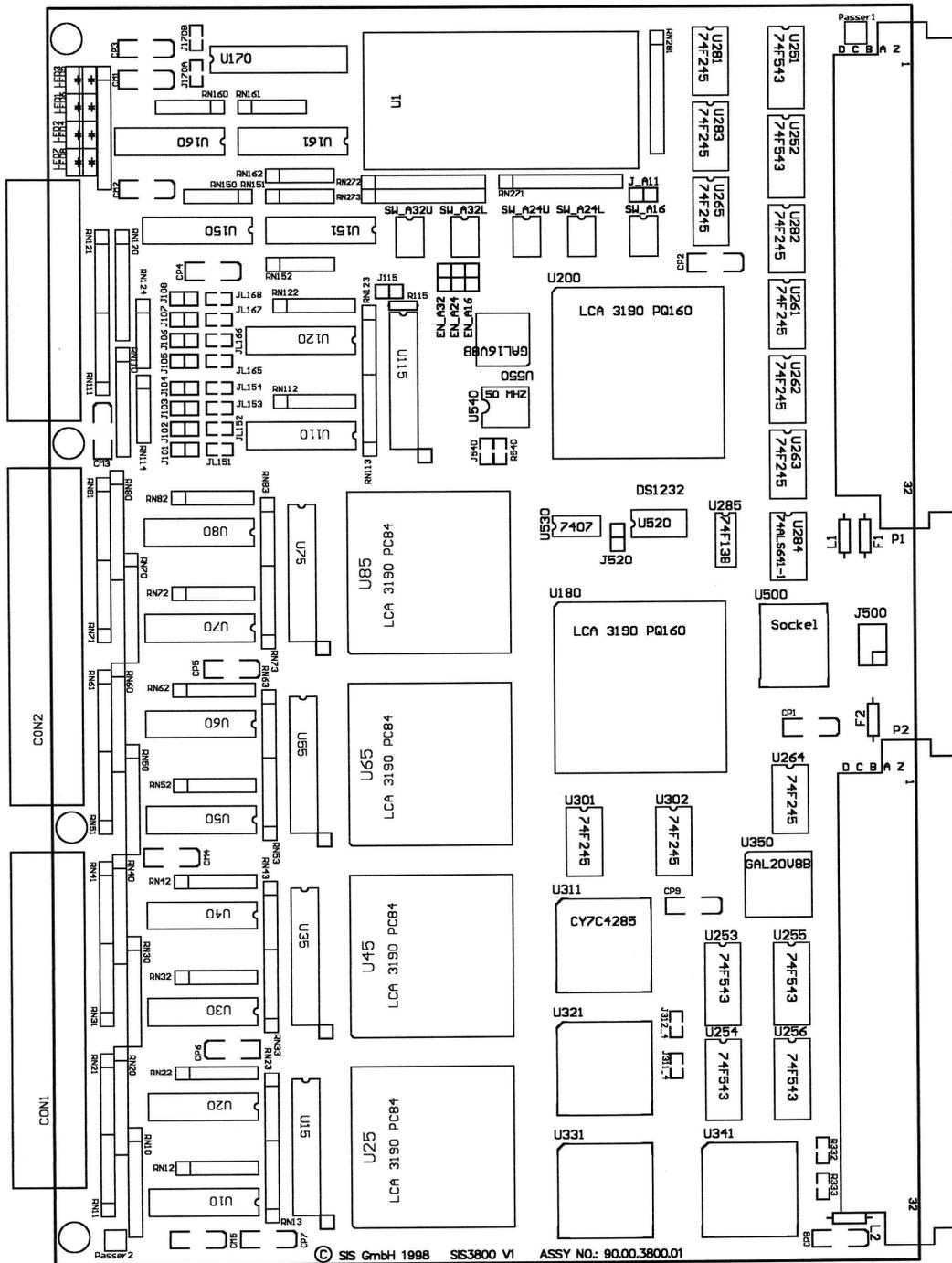
18.7 Operation notes

Due to the flexibility of the SIS3801 V5 through V8 designs the unit covers a broad range of counter based data acquisition applications. In some cases the user may find possible uses of the board we did not see (yet?) during the design, test and documentation phase, on the other hand we found possibilities, which may not be obvious to the first time user. Two of them are described below:

18.7.1 Use as pulse generator

If you do not have a programmable VME pulse generator like the SIS3807 at hand and have the need to generate fixed frequency output pulses you can use the CIP output with the following register settings:

- load the copy disable register with 1 (has the effect that no channels are copied to the FIFO, hence the unit will not run in a FIFO full condition, what would stop CIP)
- set the LNE prescaler to the desired factor (the minimum dwell time with no channel enabled is in the order of 400 ns, the CIP will occur at the maximum possible frequency if you program a lower value
- enable the 10 MHz to LNE pulser

18.7.2 Time Monitoring

If you use the external, external prescaled or channel 1 prescaled LNE source you can monitor the time between LNE signals with the 25 MHz channel 1 reference pulser. This allows you to determine the speed of a stepper motor if the motor clock is used as prescaled LNE signal to give an example.

18.7.3 Retrieve FLASHPROM contents

If you are not sure what firmware designs are actually burned into your FLASHPROM you can find out by making use of the jumper array J500 (FLASPROM file selection) and the module identification and IRQ register . Set your unit to file 0 (all jumpers set), power up the crate and read the module identification register. Proceed with selecting file 1 (lowest jumper open) and continue until the unit does not boot (module stuck in LED selftest). As we do not make FLASHPROMS with gaps in between the boot files you will have a complete listing of all files on the FLASHPROM at this point.

18.8 Cascaded FIFOs

The SIS3801 board can be stuffed with one or four synchronous FIFO chips, the standard unit comes with one 64K FIFO chip as default. The FIFO flags are handled by a PLD (programmable logic device) if four FIFO chips are installed.

The meaning of the almost empty, half full and almost full flag is redefined in this case, as these flags are derived from the status of all four FIFO chips, as data are written to and read from the FIFO chips in a ring buffer fashion.

Find below two table with the FIFO conditions for the V2 and the V3 FIFO GAL:

V2 GAL	FIFO flag	Meaning in 256K case	Condition
	empty	empty	set if empty
	almost empty	25 to 50% full	0: < 64K –128 (16-bit) words 0 or 1: between 64K –128 (16-bit) words and 128 K –256 (16-bit) words 1: >128 K –256 (16-bit) words
	half full	not used	don't care
	almost full	50 to 75% full	0: < 128K –256 (16-bit) words 0 or 1: between 128K –256 (16-bit) words and 192 K –384 (16-bit) words 1: >192 K –384 (16-bit) words
	full	full	set if full

V3 GAL	FIFO flag	Meaning in 256K case	Condition
	empty	empty	set if empty
	almost empty	25 to 50% full	0: < 64K –128 (16-bit) words 0 or 1: between 64K –128 (16-bit) words and 128 K –256 (16-bit) words 1: >128 K –256 (16-bit) words
	half full	not used	don't care
	almost full	50 to 75% full	0: < 64K –128 (16-bit) words 0 or 1: between 64K –128 (16-bit) words and 128 K –256 (16-bit) words 1: >128 K –256 (16-bit) words
	full	full	set if full

Example: If the FIFO almost empty flag is cleared, the user can read a minimum of 64K-128 (16-bit) words from the FIFO in a block transfer and has the guarantee, that he can store an additiona128 K (+256) words before running into overflow.

Note: The difference between the V2 and the V3 FIFO GAL lies in the condition of the almost full flag. As the almost empty condition itself can not be used to generate a VME interrupt, the almost empty condition is used for the almost full flag in the V3 GAL, what gives you much more time to handle the interrupt and the FIFO data. It will depend on the application, whether the V2 or V3 design is appropriate.

18.9 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from
http://www.struck.de/sis3638firm.htm. Please note, that a special hardware configuration may
be necessary for the firmware design of interest (the SIS3801 design requires the installation
of a FIFO e.g.).
The table on the web is of the format shown below:

SIS36/38xx FLASHPROM table

The table below is an excerpt form the full table, which is on the web, only.

Design Name	Design	Boot File (s)
SIS3800_201098	0	SIS3800 Version 1
SIS3801_201098	0	SIS3800 Version 1
	1	SIS3800 Version 2
	2	SIS3801 Version 1 (32-bit Design)
	3	SIS3801 Version 2 (24-bit Design)
SIS3803_280798	0	SIS3803 Version 1
SIS3801_170400	0	SIS3801 Version 5 (32-bit Design)
	1	SIS3801 Version 6 (24-bit Design)
	2	SIS3800 Version 2
	3	SIS3801 Version 9 (32-bit Design)
	4	SIS3801 Version A (24-bit Design)
	5	SIS3800 Version 3

18.10 Row d and z Pin Assignments

The SIS3801 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

18.11 Geographical Address Pin Assignments

The SIS38xx board series is prepared for geographical addressing via the geographical address pins GA0*, GA1*, GA2*, GA3*, GA4* and GAP*. The address pins are left open or tied to ground by the backplane as listed in the following table:

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

18.12 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, http://www.vita.com (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs like CERN or FNAL

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