VMIVME-3801

ISOLATED SCANNING 12-bit, 31-CHANNEL ANALOG-TO-DIGITAL CONVERTER BOARD WITH BUILT-IN-TEST (BIT) AND SCREW TERMINAL INTERFACE

PRODUCT MANUAL

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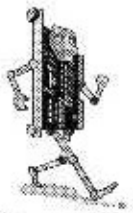

(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

RECORD OF REVISIONS

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A	05/23/95	Release	95-0357
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VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VMIC ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

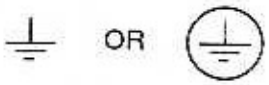
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

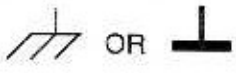
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

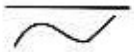
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

VMIVME-3801
ISOLATED SCANNING 12-bit, 31-CHANNEL ANALOG-TO-DIGITAL CONVERTER BOARD WITH BUILT-IN-TEST (BIT) AND SCREW TERMINAL INTERFACE

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SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-3801 Analog Input Board provides automatic scanning of 16 differential or 31 single-ended analog input channels. The channels are digitized with a 12-bit resolution Analog-to-Digital Converter (ADC). Each input is overvoltage protected and low pass filtered. The board is very easy to use, no software setup is required. After power up or system reset, the VMIVME-3801 automatically starts scanning each of its 16 or 31 input channels. Conversion data is stored automatically in dual-port memory (RAM), making it immediately accessible from the VMEbus. The VMIVME-3801 provides on-board voltage references to perform an on-line or off-line built-in self-test. The input voltage range and gain are user-configurable jumpers. The VMEbus base address and the access mode are fully selectable. In short I/O space, the board can be ordered to support optional current inputs (0 to 25 mA) using 31-channel single-ended inputs.

Some of the distinguishing features of the VMIVME-3801 include:

a. VMEbus 6U single height format
b. 16 differential or 31 single-ended analog input channels
c. One 12-bit A/D Converter with built-in track-and-hold
d. Automatic scanning of all inputs at 40 kHz aggregate rate
e. No software initialization required to begin scanning
f. Input ranges from ±50 mV to ±10 VDC
g. Input overvoltage protection
h. Analog inputs are low pass filtered at 50 kHz
i. Optional add-on 40 Hz low pass filter card
j. Discrete wire cables
k. Input pull-down resistors prevent floating inputs
l. Supports on-line and off-line Built-in-Test (BIT)
m. Configurable jumper gains of x1, x10, x100
n. Selectable A/D ranges of ±5 VDC, ±10 VDC, and 0 to 10 VDC
o. Data Accesses: D16, D08(EO), D08(O)
p. Front panel LED
q. 1,000 VDC isolation between analog and digital ground
r. Optional 0 to 20, 4 to 20, and 5 to 25 mA current input range

The VMIVME-3801 occupies 128 bytes of short I/O VMEbus addressing space. Jumpers are provided to place the board on any 128-byte boundary. The board can also be jumpered to respond to supervisory, nonprivileged, or both accesses.

Conversion data is available from a 16-bit register (12-bit right-justified with optional sign extension). This data is stored in on-board dual-ported memory (RAM) for easy access.

The Built-in-Test (BIT) gives the user the capability to verify the on-board ADC using high precision, user-programmable reference voltages. Software controls the BIT functions.

After a system reset, the board returns to a fixed configuration: all bits in the Control/Status Register are cleared and the front panel FAIL LED is illuminated. The LED is then extinguished under software control. This LED can be used to visually locate a faulty board in a system.

1.2 REFERENCE MATERIAL LIST

Refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA

VMEbus International Trade Association

7825 East Gelding Drive

Suite 104

Scottsdale, AZ 85260-3415

(602) 951-8866

FAX: (602) 951-0720

Internet: www.vita.com

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006
Data Aquisition Noise Reduction Application Guide	825-000000-026

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003801-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3801 is a flexible, low-cost analog input board that provides 16 differential or 31 single-ended analog input channels. The channels are scanned continuously at an aggregrate rate of 40 kHz using a 12-bit resolution Analog-to-Digital Converter (ADC). Channels can randomly or sequentially read at any time. The current address of the channel being digitized is read from the Channel Pointer Register. Scanning may be halted at the current channel using the Stop Auto Scan bit in the Control/Status Register. This will disable further channel address increments. The board will then lock onto that channel. This allows a single channel to be digitized every 25 µs. The following sections discuss the functional components of the VMIVME-3801 in detail.

3.2 FUNCTIONAL ORGANIZATION

The VMIVME-3801 is divided into the following functional categories. Each category is discussed in detail.

a. VMEbus Interface

b. Analog-to-Digital Converter (ADC) and Control Logic

c. Analog Input Multiplexing, Gain, and Conversion

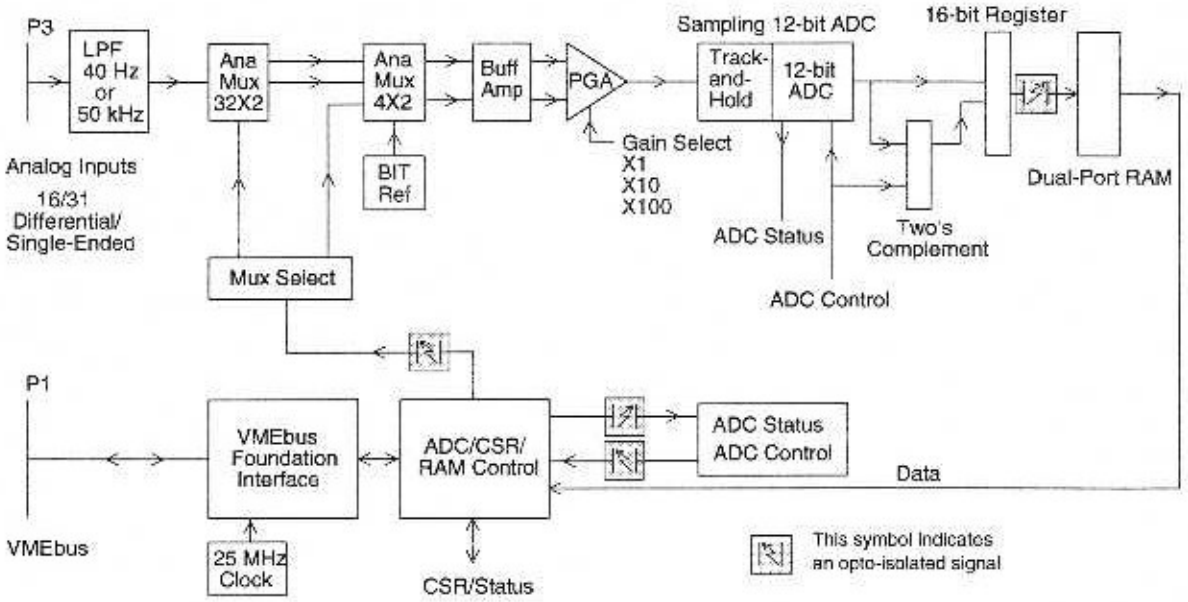
d. BIT Voltage Reference and multiplexer

e. Board ID register

Figure 3.2-1 on page 3-2 illustrates the functional blocks of the VMIVME-3801.

3.3 VMEbus INTERFACE

The VMIVME-3801 communication registers are memory mapped as 64 16-bit words (128 bytes) in memory. The registers are contiguous and may be located on any 128-byte boundary within the short I/O space of the VMEbus. The board can be configured to respond to short supervisory or short nonprivileged data accesses, or both. See Section 5 for address jumper locations and configurations.



M3801/F3.2-1

Figure 3.2-1. VMIVME-3801 Functional Block Diagram

During each read or write operation, all VMEbus control signals are ignored, unless the board selection comparator detects a match between the on-board selection jumpers and the address and address modifier line from the backplane. The appropriate board response occurs if a valid match is detected. The open-collector DTACK* interface signal is then asserted (driven low). Subsequent completion of the bus master's read or write cycle causes the board-generated DTACK* signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communication with the board. They are as follows:

a. Data bus lines D00 to D15
b. Address lines A01, A02, A03, A04, A05, A06, A07
c. Bus Control Signals:
   Write
   DS0*, DS1*
   SYSCLK
   SYSRESET*

Data bus lines are bidirectional and move data to and from the board through a 16-bit data transceiver responding to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A07 map the 64 registers into 128-byte range within the VMEbus address space described in Section 4. The control signals determine whether data is to be moved *to* the board (write) or *from* the board (read). The control signals also provide the necessary data strobes (DS0,DS1). A SYSRESET input resets all CSR bits.

Static controls are latched into the Control Register and are used primarily to establish the operational mode of the board.

3.4 ANALOG-TO-DIGITAL CONTROL AND TIMING

Control commands and status flags associated with controlling the Analog-to-Digital Converter (ADC) are described in Section 4.

There are two modes of operation for this board. The first is to continuously scan all 16 or 31 analog input channels. The second is to halt scanning and lock onto a single channel. Either way, the electrical process of A/D conversion is similar.

The VMIVME-3801 uses a 12-bit ADC. The ADC has a conversion time of 8.5 µs. Settling time is required for the multiplexers and the Programmable Gain Amplifier (PGA) before the ADC cycle may begin. The total channel acquisition cycle occurs every 25 µs. All conversion timing is provided by internal sources. This gives an aggregate scan rate for all channels of 40 kHz. The ADC's built-in track-and-hold amplifier prevents signals that vary during a conversion cycle from giving false ADC readings.

After the multiplexer and gain amp have settled, the ADC is placed into the convert mode. The ADC BUSY signal then goes active high to indicate the ADC is currently working on a new conversion cycle. The internal track-and-hold automatically changes from the track to the hold mode, the ADC then begins its successive approximation conversion cycle. The conversion digitizes the analog signal from the track-and-hold amp into a 12-bit data word.

The ADC signals the completion of its cycle by lowering the BUSY signal to a logic "0". If the Two's Complement bit is set in the CSR, the ADC's 12-bit output is modified into two's complement format. At this point, the 12-bit word is latched for storage to the dual-port RAM.

3.5 BUILT-IN-TEST REFERENCE

The board is equipped with a programmable precision voltage reference which can be used as a Built-in-Test (BIT) of the board. When selected, the BIT voltage is fed through the Programmable Gain Amplifier (PGA) to the Analog-to-Digital Converter (ADC) bypassing the external analog input on channel zero. Therefore, the channel zero location in the dual-port RAM will be written with the BIT voltage's equivalent digital value. After enabling the BIT voltage (Mode 0 bit set), the user should wait for enough time to elapse (810 μs maximum), to allow sequencing through channel zero before checking its value. The BIT is used to test the PGA, the ADC, and the dual-port RAM memory. The BIT can be enabled at any time during initial board installation or in real time for system self-diagnostics.

The BIT reference is selected from one of three internal precision reference voltages: +4.980 VDC, +0.4928 VDC, +9.915 mVDC, or analog ground (0.0 VDC).

The selection is provided by setting the Mode bits 0, 1, and 2 in the CSR according to the Control/Status Register detailed in Section 4.

If mode bit zero is a logical "0," the board scans all 16 or 32 channels in a normal mode of operation. If the mode bit is set in the CSR , channel zero corresponds to the selected reference voltage VREF0, VREF1, VREF2, or Analog Ground according to the settings of Mode bit 1 and Mode bit 2. The digital value received should be within ±10 LSBs of the selected reference voltage. The remaining channels (1-15 or 1-31) digitize their respective external input sources. Thus, channel zero may be periodically checked during run time to verify the ADC operation. Please note that the current gain and unipolar/bipolar modes must be considered when selecting the reference voltage. The BIT voltage precedes the PGA and multiplies the selected reference voltage. Selecting a reference voltage which exceeds the ADC range when multiplied by the gain amplifier is not recommended.

3.6 ANALOG INPUTS

There is either 16 differential or 31 single-ended analog inputs available on the front panel connector. VMIC recommends that the differential mode be used for decreased noise, greater common-mode rejection, and improved accuracy. Unused inputs should be grounded, including the low side of all unused differential inputs. The board has internal 22 MΩ pull-down resistors on the low side of the differential inputs. This prevents the differential input pair from drifting up past the input multiplexers' maximum voltage limit.

NOTE:

WHEN CONFIGURED FOR SINGLE-ENDED MODE, CHANNEL 31 IS JUMPER CONFIGURABLE AS A COMMON GROUND BY INSTALLING E17.

3.6.1 Low Pass Filters

The VMIVME-3801 provides passive single pole low pass input filters on all inputs. The normal -3 dB cut off frequency is 50 kHz. This provides some high frequency noise protection for the board. The board can also be configured with an add-on daughter board option. The daughter board provides a low pass filter with a cut off frequency of 40 Hz. This lower cut off frequency provides protection from local 60 Hz AC line noise. This option is normally installed by the factory at the time of order. It can be removed by the user at a later date if new applications arise. If the board is running in single-ended mode, the user must install the two 0 Ω SIP jumpers in locations J4 and J5. This allows the low pass filter to perform in the single-ended configuration. Note that the VMIVME-3801 requires a jumper change if the 40 Hz daughter board is added.

3.6.2 Input Multiplexers

The board has two tiers of analog multiplexing. Each of the 32 inputs is selected using one of four 8 X 1 first-tier analog input multiplexers. The second-tier multiplexer is configured as a 4 X 2 board. It selects one or two of the first-tier output signals to provide the single-ended or differential mode of operation. The second-tier multiplexer also selects the BIT reference voltage, if enabled in the Control/Status Register. The second-tier output is differentially transferred to the Programmable Gain Amplifier (PGA).

3.6.3 Current Inputs

The VMIVME-3801-2BC and -3BC models include current termination resistors using a daughter board installed in the place of the 40 Hz filter. This allows a current signal to be terminated to ground. The voltage developed across a resistor is read by the VMIVME-3801. The optional -2BC board resistors value at 250 Ω ±0.01 percent. The optional -3BC board provides resistor value at 500 Ω ±0.01 percent. To support this option the 50 kHz low pass filter is not installed at the factory, all other functionality of the board remains the same.

NOTE:

THE OPTIONAL -2BC AND -3BC BOARDS ARE CONFIGURED FOR 31-CHANNEL SINGLE-ENDED MODE ONLY. DIFFERENTIAL INPUTS ARE NOT SUPPORTED.

3.7 PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

Once an input channel has been selected and routed through the input multiplexers, it enters the PGA as a differential input. The differential amplifier rejects common-mode noise and delivers a scaled, single-ended output to the ADC. The PGA

may be hardware jumpered for gains of 1, 10, and 100. This allows for inputs as low as ±50 mV up to ±10 VDC in range. There is no increase in acquisition time for any change in the gain setting.

3.8 CHANNEL SEQUENCER AND DUAL-PORTED RAM MEMORY

The VMIVME-3801 is normally operated in the scanning mode. When the board is powered up or reset, conversions start immediately. Once the A/D conversion is completed, the dual-port control logic takes the converted data and stores it in the channel's appropriate dual-port register. The channel counter is incremented by one. This selects the next channel to be multiplexed to the ADC. After selecting the next channel, a new A/D conversion sequence is initiated. When all input channels have been converted and stored (16 or 32), the channel counter is reset and starts the channel scanning sequence again.

The Stop Auto Scan bit in the Control/Status Register (CSR) may be set to halt the channel sequencer at its current address. This address can be read from the Channel Pointer Register. This feature allows the controlling software to lock onto a channel and digitize it at the maximum rate of 40 kHz. Please note that the channel desired can not be directly set. The software must wait for the desired channel to appear in the Channel Pointer register to set the Stop Auto Scan bit within 25 µs.

3.9 BOARD ID REGISTER

The first location in the VMIVME-3801 register set is a read-only Board ID Register. It always reads $44. Other VMIC products have similar registers which read different constants. This allows general-purpose system software to automatically determine what boards have been installed.

3.10 BUILT-IN POWER CONVERTER AND ADC POWER SUPPLY

Electrical power for the VMIVME-3801 analog circuitry is supplied by an on-board DC-to-DC Converter. The converter transforms +5 VDC power from the VMEbus into a regulated ±15 VDC power. The VMIVME-3801 does not require any 12 VDC from the VMEbus.

The ADC's +5 VDC logic power is provided by an on-board voltage regulator. Some of the +15 VDC from the DC-to-DC converter's output is used as the input voltage to this regulator.

In addition to the ±15 V DC-to-DC converter, the VMIVME-3801 uses a separate +5 V DC-to-DC Converter to provide an isolated analog ground for the ADC.

SECTION 4

PROGRAMMING

4.1 MEMORY MAP

The VMIVME-3801 occupies 128 bytes of addressing space including four information and control registers plus the conversion data registers. Tables 4.1-1 through 4.1-3 map this addressing space relative to the base address as set by configuration jumpers (see Section 5 for details concerning setting the base address and address modifier jumpers).

The appropriate table is determined by two factors: whether the board is jumpered for single-ended or differential inputs, and whether the user has selected the normal or maximum data buffer for differential inputs. If the board is jumpered for differential inputs and the Max Buffer bit in the Control/Status Register (CSR) is clear, Table 4.1-1 applies. If the board is jumpered for differential inputs and the Max Buffer bit is set, Table 4.1-2 applies. If the board is jumpered for single-ended inputs, Table 4.1-3 is the only map that applies (see Section 5 for setting the input configuration jumpers).

Table 4.1-1. VMIVME-3801 Memory Map: Differential Inputs, Normal Buffer

OFFSET ADDRESS	FUNCTION	MNEMONIC	WIDTH	ACCESS
$00	BOARD ID REGISTER	BIR	BYTE	READ-ONLY
$01	CONFIGURATION REGISTER	BCR	BYTE	READ-ONLY
$02	CONTROL/STATUS REGISTER	CSR	BYTE	READ/WRITE
$03	CHANNEL POINTER REGISTER	CPR	BYTE	READ-ONLY
$04-$3F	RESERVED			
$40	CHANNEL 0 DATA	CH0	WORD	READ/WRITE
$42	CHANNEL 1 DATA	CH1	WORD	READ/WRITE
$44	CHANNEL 2 DATA	CH2	WORD	READ/WRITE
$46	CHANNEL 3 DATA	CH3	WORD	READ/WRITE
$48	CHANNEL 4 DATA	CH4	WORD	READ/WRITE
$4A	CHANNEL 5 DATA	CH5	WORD	READ/WRITE
$4C	CHANNEL 6 DATA	CH6	WORD	READ/WRITE
$4E	CHANNEL 7 DATA	CH7	WORD	READ/WRITE
$50	CHANNEL 8 DATA	CH8	WORD	READ/WRITE
$52	CHANNEL 9 DATA	CH9	WORD	READ/WRITE
$54	CHANNEL 10 DATA	CH10	WORD	READ/WRITE
$56	CHANNEL 11 DATA	CH11	WORD	READ/WRITE
$58	CHANNEL 12 DATA	CH12	WORD	READ/WRITE
$5A	CHANNEL 13 DATA	CH13	WORD	READ/WRITE
$5C	CHANNEL 14 DATA	CH14	WORD	READ/WRITE
$5E	CHANNEL 15 DATA	CH15	WORD	READ/WRITE
$60-$7E	RESERVED			

M3801/T4.1-1

Table 4.1-2. VMIVME-3801 Memory Map: Differential Inputs, Maximum Buffer

OFFSET ADDRESS	FUNCTION	MNEMONIC	WIDTH	ACCESS
$00	BOARD ID REGISTER	BIR	BYTE	READ-ONLY
$01	CONFIGURATION REGISTER	BCR	BYTE	READ-ONLY
$02	CONTROL/STATUS REGISTER	CSR	BYTE	READ/WRITE
$03	CHANNEL POINTER REGISTER	CPR	BYTE	READ-ONLY
$04-S3F	RESERVED			
$40	CHANNEL 0 DATA	CH0	WORD	READ/WRITE
$42	CHANNEL 1 DATA	CH1	WORD	READ/WRITE
$44	CHANNEL 2 DATA	CH2	WORD	READ/WRITE
$46	CHANNEL 3 DATA	CH3	WORD	READ/WRITE
$48	CHANNEL 4 DATA	CH4	WORD	READ/WRITE
$4A	CHANNEL 5 DATA	CH5	WORD	READ/WRITE
S4C	CHANNEL 6 DATA	CH6	WORD	READ/WRITE
$4E	CHANNEL 7 DATA	CH7	WORD	READ/WRITE
S50	CHANNEL 8 DATA	CH8	WORD	READ/WRITE
S52	CHANNEL 9 DATA	CH9	WORD	READ/WRITE
S54	CHANNEL 10 DATA	CH10	WORD	READ/WRITE
S56	CHANNEL 11 DATA	CH11	WORD	READ/WRITE
S58	CHANNEL 12 DATA	CH12	WORD	READ/WRITE
$5A	CHANNEL 13 DATA	CH13	WORD	READ/WRITE
S5C	CHANNEL 14 DATA	CH14	WORD	READ/WRITE
$5E	CHANNEL 15 DATA	CH15	WORD	READ/WRITE
$60	CHANNEL 0 DATA	CH0	WORD	READ/WRITE
$62	CHANNEL 1 DATA	CH1	WORD	READ/WRITE
$64	CHANNEL 2 DATA	CH2	WORD	READ/WRITE
$66	CHANNEL 3 DATA	CH3	WORD	READ/WRITE
$68	CHANNEL 4 DATA	CH4	WORD	READ/WRITE
$6A	CHANNEL 5 DATA	CH5	WORD	READ/WRITE
$6C	CHANNEL 6 DATA	CH6	WORD	READ/WRITE
$6E	CHANNEL 7 DATA	CH7	WORD	READ/WRITE
$70	CHANNEL 8 DATA	CH8	WORD	READ/WRITE
$72	CHANNEL 9 DATA	CH9	WORD	READ/WRITE
$74	CHANNEL 10 DATA	CH10	WORD	READ/WRITE
$76	CHANNEL 11 DATA	CH11	WORD	READ/WRITE
$78	CHANNEL 12 DATA	CH12	WORD	READ/WRITE
$7A	CHANNEL 13 DATA	CH13	WORD	READ/WRITE
$7C	CHANNEL 14 DATA	CH14	WORD	READ/WRITE
$7E	CHANNEL 15 DATA	CH15	WORD	READ/WRITE

M3801/T4.1-2

Table 4.1-3. VMIVME-3801 Memory Map: Single-Ended Inputs

OFFSET ADDRESS	FUNCTION	MNEMONIC	WIDTH	ACCESS
$00	BOARD ID REGISTER	BIR	BYTE	READ-ONLY
$01	CONFIGURATION REGISTER	BCR	BYTE	READ-ONLY
$02	CONTROL/STATUS REGISTER	CSR	BYTE	READ/WRITE
$03	CHANNEL POINTER REGISTER	CPR	BYTE	READ-ONLY
$04-$3F	RESERVED			
$40	CHANNEL 0 DATA	CH0	WORD	READ/WRITE
$42	CHANNEL 1 DATA	CH1	WORD	READ/WRITE
$44	CHANNEL 2 DATA	CH2	WORD	READ/WRITE
$46	CHANNEL 3 DATA	CH3	WORD	READ/WRITE
$48	CHANNEL 4 DATA	CH4	WORD	READ/WRITE
$4A	CHANNEL 5 DATA	CH5	WORD	READ/WRITE
$4C	CHANNEL 6 DATA	CH6	WORD	READ/WRITE
$4E	CHANNEL 7 DATA	CH7	WORD	READ/WRITE
$50	CHANNEL 8 DATA	CH8	WORD	READ/WRITE
$52	CHANNEL 9 DATA	CH9	WORD	READ/WRITE
$54	CHANNEL 10 DATA	CH10	WORD	READ/WRITE
$56	CHANNEL 11 DATA	CH11	WORD	READ/WRITE
$58	CHANNEL 12 DATA	CH12	WORD	READ/WRITE
$5A	CHANNEL 13 DATA	CH13	WORD	READ/WRITE
$5C	CHANNEL 14 DATA	CH14	WORD	READ/WRITE
$5E	CHANNEL 15 DATA	CH15	WORD	READ/WRITE
$60	CHANNEL 16 DATA	CH16	WORD	READ/WRITE
$62	CHANNEL 17 DATA	CH17	WORD	READ/WRITE
$64	CHANNEL 18 DATA	CH18	WORD	READ/WRITE
$66	CHANNEL 19 DATA	CH19	WORD	READ/WRITE
$68	CHANNEL 20 DATA	CH20	WORD	READ/WRITE
$6A	CHANNEL 21 DATA	CH21	WORD	READ/WRITE
$6C	CHANNEL 22 DATA	CH22	WORD	READ/WRITE
$6E	CHANNEL 23 DATA	CH23	WORD	READ/WRITE
$70	CHANNEL 24 DATA	CH24	WORD	READ/WRITE
$72	CHANNEL 25 DATA	CH25	WORD	READ/WRITE
$74	CHANNEL 26 DATA	CH26	WORD	READ/WRITE
$76	CHANNEL 27 DATA	CH27	WORD	READ/WRITE
$78	CHANNEL 28 DATA	CH28	WORD	READ/WRITE
$7A	CHANNEL 29 DATA	CH29	WORD	READ/WRITE
$7C	CHANNEL 30 DATA	CH30	WORD	READ/WRITE
$7E	CHANNEL 31 DATA	CH31	WORD	READ/WRITE

M3801/T4.1-3

4.2 REGISTER DESCRIPTIONS

The VMIVME-3801 control registers are all byte-wide registers, while the data registers are all 16 bits wide. The control registers can also be accessed as 16-bit words, in which case two successive registers are accessed.

NOTE:

ALL BITS DOCUMENTED AS "RESERVED" READ AS ZERO AND, IF WRITTEN, MUST ALWAYS BE WRITTEN AS ZERO.

4.2.1 Board ID Register

The VMIVME-3801 Board ID Register is an 8-bit, read-only register at offset $00 with a constant value set at $44. This ID number uniquely identifies the board from other VMIC products.

Table 4.2.1-1. Board ID Register Bit Map

BOARD ID REGISTER (OFFSET $00) READ-ONLY, BYTE							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
0	1	0	0	0	1	0	0

M3801/T4.2.1-1

4.2.2 Board Configuration Register

The Configuration Register is an 8-bit, read-only register at offset $01. It indicates the current configuration of the VMIVME-3801 board. It contains two bits of configuration status information, each determined by jumper configuration on the board. See Table 4.2.2-1 for the location of these bits. The Input Mode bit (bit 0) indicating single-ended or differential operation is controlled by a jumper (E5) and can be set as desired (jumper E5 installed: ON = logical "0" differential, E5 omitted: OFF = logical "1" single-ended). The frequency bit (bit 1) is controlled by jumper (E6) on the board. With jumper E6 installed: ON = logical "1" 40 Hz, and E6 omitted: OFF = logical "0" 50 kHz. This allows the user to check for the installed filter.

Table 4.2.2-1. Board Configuration Register Bit Map

BOARD CONFIGURATION REGISTER (OFFSET $01) READ-ONLY, BYTE							
BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FREQ (E6)	INPUT MODE (E5)

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NOTE:

FOR THE -2BC AND -3BC CURRENT OPTIONS, THE BIT POSITIONS ARE SHOWN AS FOLLOWS:

- **BIT POSITION 1 = 0, INDICATING THE CURRENT TERMINATION RESISTOR BOARD IS NOT INSTALLED**
- **BIT POSITION 1 = 1, INDICATING THE TERMINATION BOARD IS INSTALLED**

4.2.3 Control/Status Register (CSR)

The Control/Status Register (CSR) is an 8-bit read/write register at offset $02 that allows software to control the VMIVME-3801 and indicate its current status. Seven of the eight bits provide control and indication functions. Table 4.2.3-1 show the contents of this register.

Table 4.2.3-1. Control/Status Register Bit Map

CONTROL/STATUS REGISTER (OFFSET $02) READ/WRITE, BYTE							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
LED OFF	RESERVED	MODE 2	MODE 1	MODE 0	2'S COMPL	MAX BUFFER	STOP AUTO SCAN

(X = Don't Care)

Power-up/Reset Default = $0000

M3801/T4.2.3-1

Control/Status Register Bit Definitions

Bit 15: LED Off - The front panel LED is ON by default and normally turned OFF after power up or reset by the host software. The LED can be used to visually verify that the board has been initialized. A logical "1" in this bit position turns the LED OFF, a logical "0" turns the LED ON.

Bit 14: Reserved - Forced to zero

Bits 13-11: Mode[2:0] - These bits offer the user the capability to apply a selected voltage to channel zero for calibration and self-check. The three Mode bits determine the stimulus to channel zero, according to Table 4.2.3-2.

Table 4.2.3-2. Board Control/Status Register: Modes

MODE 2	MODE 1	MODE 0	CHANNEL 0 STIMULUS
X	X	0	EXTERNAL INPUT (DEFAULT)
1	1	1	INTERNAL 0.000 V REFERENCE
1	0	1	INTERNAL 9.915 mV REFERENCE
0	1	1	INTERNAL 492.8 mV REFERENCE
0	0	1	INTERNAL 4.980 V REFERENCE

M3801/T4.2.3-2

Bit 10: Two's COMPL - If the Two's Complement bit is set (logical "1"), all information in the Data Registers will be in Two's Complement format. This data format is only useful when the inputs are configured as bipolar, in which case the Two's Complement data format causes the Data Registers to contain values already sign-extended. This saves the programmer from having to convert the data in the host code, otherwise data is read as binary.

Bit 9: MAX Buffer - The Max Buffer bit is only significant when the hardware is configured for differential inputs. It controls whether there are 16 Data Registers (one for each input) or 32 Data Registers (two for each input). The user can set the Max Buffer bit to "buy some time" by extending the aggregate sample time from just under 500 µs to nearly a millisecond. By setting the Max Buffer bit, all 32 Data Registers are updated; data for channels 0-15 is stored consecutively, first in the lowest 16 Data Registers (channel 0 data at offset $40), then in the higher 16 Data Registers (channel 0 data at offset $60).

Bit 8: Stop Auto Scan - Normally, the VMIVME-3801 automatically scans all input channels, continually converting each successive input. The user can set the Stop Auto Scan bit, causing the VMIVME-3801 to stop on a single channel. If the Stop Auto Scan bit is set, only the Data Register pointed to by the Channel Pointer Register is updated. The Data Register is updated much faster than usual – approximately every 25 µs. The best way to stop on a single desired channel for close monitoring is to observe the Channel Pointer Register while autoscanning. Set the Stop Auto Scan bit within 25 µs as soon as the desired channel appears. Auto scanning proceeds from the current channel as soon as this bit is cleared again.

4.2.4 Channel Pointer Register (CPR)

The Channel Pointer Register is an 8-bit read-only register at offset $03. Under most circumstances, the Channel Pointer Register holds the channel number of the current input being sampled and converted by the VMIVME-3801. The only exception occurs when the board is configured for differential input and the Max Buffer bit in the Control/Status Register is set. In this case, two data pages get updated so that each input is converted in two separate passes. The Channel Pointer Register can be used to determine which of the two Data Registers has been recently updated. The offset address of the Data Register being converted may be calculated as follows:

(Channel Pointer Register value x 2) + $40 = Offset Address of Current Data Register

Note that the corresponding channel number is simply the Channel Pointer Register value modulo 16. Also note that the value in this register represents the current channel under conversion. Decrement the value by one (modulo 16 for differential inputs or 32 for single-ended inputs) to determine the location of the most recently completed channel data. Table 4.2.4-1 is an example.

Table 4.2.4-1. Example: Channel Pointer Register (CPR) Bit Map

CHANNEL POINTER REGISTER (OFFSET $03) READ-ONLY, BYTE							
BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
0	0	0	0	1	1	1	0

M3801/T4.2.4-1

Explanation of Table 4.2.4-1 using the above equation: ($EX2) + $40 = offset 5C

4.2.5 Data Registers

There are either 16 or 32 Data Registers beginning at offset $40, depending on the condition of the Max Buffer bit. The Max Buffer bit is only significant when the hardware is configured for differential inputs. It controls whether there are 16 Data Registers (one for each input) or 32 Data Registers (two for each input). Each Data Register contains 12 bits of conversion data for its associated channel. The data is right-justified within each 16-bit Data Register. Each register should generally be treated as read-only, and accessed as a 16-bit word. The hardware does not restrict the user from accessing the Data Registers via two consecutive byte reads.

When accessing the Data Registers as bytes, it is possible for the value in the Data Register being read to be updated between byte reads, potentially scrambling the perceived data. Section 4.5 provides methods to avoid scrambled byte data reads.

The data is a linear binary representation of the input voltage on the corresponding channel at the time of the most recent conversion. The LSB weight (that is, the voltage value corresponding to a single bit of data) depends on the input voltage range which, in turn, depends on the range and gain jumper configuration (see Section 5 for details). Calculate the LSB weight by dividing the full-scale range by 4096. For example, the LSB weight for a VMIVME-3801 configured for ±10 V at unity gain would be 4.88 mV (20/4096). Table 4.2.5-1 lists the LSB weights for all possible VMIVME-3801 configurations.

Table 4.2.5-1. LSB Weight

VOLTAGE RANGE	LSB WEIGHT		
	GAIN X1	GAIN X10	GAIN X100
±5 V	2.441 mV	.2441 mV	24.41 µV
±10 V	4.883 mV	.4883 mV	48.83 µV
0-10 V	2.441 mV	.2441 mV	24.41 µV

M3801/T4.2.5-1

The voltage on any channel can be determined by multiplying the Data Register value (converted to decimal) by the appropriate LSB Weight from Table 4.2.5-1.

Two other values are very important in determining the meaning of the values in the Data Registers: the Channel Pointer Register and the Max Buffer bit, both previously described. The Channel Pointer Register holds the channel number of the Data Register currently being updated, therefore the most recent complete conversion data is for the channel one less than the value of the Channel Pointer Register (modulo 32 or 16, depending upon the number of active Data Registers).

The Max Buffer bit in the Control/Status Register determines whether there are 16 or 32 active differential data registers. If the bit is set, all 32 registers are actively updated, but if the bit is clear, only the first 16 registers are updated.

If the board is configured for single-ended inputs (i.e., if the Single-Ended bit in the Configuration Register is set), then the Max Buffer bit is meaningless. In this configuration, the 32 Data Registers contain the data for channels 0-31 consecutively, beginning with channel 0 at offset $40. If the board is configured for differential inputs (i.e., if the Single-Ended bit in the Configuration Register is clear), then the Max Buffer bit can be either set or cleared, depending on the user's wishes. The trade-off is between simplicity of access (Max Buffer bit clear; 16 Data Registers) and relaxed access requirements (Max Buffer bit set; 32 Data Registers).

By clearing the Max Buffer bit, only the first 16 Data Registers are updated, corresponding to channels 0-15 consecutively, beginning with channel 0 at offset $40. This is the simplest configuration, but it may require more bus overhead than desired if the user wishes to avoid constantly reading the board but still wants to capture every single data sample.

The user can set the Max Buffer bit to "buy some time" by extending the aggregate sample time from just under 500 µs to nearly a millisecond. By setting the Max Buffer bit, all 32 Data Registers are updated; data for channels 0-15 is stored consecutively, first in the lowest 16 Data Registers (channel 0 data at offset $40), then in the higher 16 Data Registers (channel 0 data at offset $60). Thus, using this technique, the two most recent scans are always available in the Data Registers. The Channel Pointer Register must be read to determine which of the two data sets is most recent: in this case, the Channel Pointer Register value does not hold a channel number, but rather an offset value into the extended data buffer. The code must still be structured such that the previously updated data is read prior to being overwritten by new data.

Note that the Data Registers are actually writable. Since the registers physically consist of RAM, writes are allowed to facilitate testing of the data RAM. Unless autoscanning is halted, however, any data written to a Data Register is overwritten with new data the next time that channel is scanned and converted.

4.3 BUILT-IN-TEST FUNCTIONS (BIT)

The VMIVME-3801 has the ability to test its functionality by applying various internal reference voltages to the channel zero input. Host software can then read the value for channel zero and compare it to its predicted quantity. Tables 4.3-1 through 4.3-3 show all possible BIT values.

Table 4.3-1. BIT Values for 0 through 10 V Range

BIT VOLTAGE	GAIN SETTING		
	X 1	X 10	X 100
0.000 V	$0000	$0000	$0000
9.915 mV	$0004	$0028	S0196
492.8 mV	$00C9	$07E2	$0FFF
4.980 V	$07F8	$0FFF	$0FFF

Table 4.3-2. BIT Values for ±5 V Range

BIT VOLTAGE	GAIN SETTING		
	X 1	X 10	X 100
0.000 V	$0800	$0800	$0800
9.915 mV	$0804	$0828	$0996
492.8 mV	$08C9	$0FE2	S0FFF
4.980 V	S0FF8	S0FFF	S0FFF

Table 4.3-3. BIT Values for ±10 V Range

BIT VOLTAGE	GAIN SETTING		
	X 1	X 10	X 100
0.000 V	$0800	S0800	$0800
9.915 mV	$0802	S0814	$08CB
492.8 mV	$0864	$0BF1	$0FFF
4.980 V	$0BFB	$0FFF	$0FFF

M3801/T4.3-1 through 4.3-3

Of course, these tables assume precisely calibrated BIT reference voltages. Check the specification for exact tolerances of these voltages. Note also that these tables assume pure binary data. The Two's Complement bit in the Control/Status Register must be clear. Any value of $0FFF indicates an overvoltage condition.

4.4 RANGE AND GAIN DETERMINATION

While the VMIVME-3801 analog gain and range can be set by the user, there is no direct way to read these settings in software (see Section 5 for hardware gain and range configuration). Software can apply a BIT voltage stimulus and attempt to determine the current gain and range settings by comparing the data to the values in Tables 4.3-1 through 4.3-3. This technique is not recommended, since the board must be calibrated to a single gain and range setting.

4.5 ACCESSING DATA AS BYTES

As stated in the Data Register description (Section 4.2.5), the Data Registers are generally accessed using single 16-bit word transfers. It is possible to access a Data Register using two successive byte transfers; however, be aware of the risk involved. The data as interpreted by the host can be completely scrambled if the VMIVME-3801 happens to update the Data Register in between the two-byte accesses. There are two methods to avoid this:

One method uses the Halt bit in the Control/Status Register to temporarily suspend automatic scanning while the two bytes are being read. Valid data can be guaranteed by carefully monitoring the Channel Pointer Register to avoid accessing channel data that is currently being converted or is about to be converted and temporarily stopping all conversions with the Halt bit in the Control/Status Register. Once scanning is halted, any Data Register can be safely read as bytes except for the Data Register pointed to by the Channel Pointer Register. The drawbacks to such a method are that it is inherently slow and the user loses a regular time reference, since the clock is essentially stopped while the Halt bit is set. (That is, the data is frozen for all channels except the one pointed to by the Channel Pointer Register, whose input gets converted constantly.)

The other method to read the Data Registers as bytes avoids interrupting the regular automatic scanning process (and thus preserves the conversion frequency of all channels). This method requires the user to structure the code so that the two-byte accesses are guaranteed to be consecutive and uninterrupted. The Channel Pointer Register must be monitored, and interrupts disabled to avoid accessing a Data Register while the data is being updated – preferably one should access a channel immediately after it has been updated. Interrupts should always be disabled before accessing a Data Register to avoid a long interrupt service routine coming between the two-byte accesses.

Of course, there are no problems or concerns if the Data Registers are accessed as a single word as recommended. For reference, however, the MSB of the data is in the lower byte address, while the LSB is in the higher byte address.

4.6 CURRENT INPUT -2BC AND -3BC OPTIONS

The -2BC option provides the current signal a 250 Ω ±0.01 percent, path to ground. The -3BC option provides the current signal a 500 Ω ±0.01 percent, path to ground.

Table 4.6-1 shows the voltages seen by the ADC.

Table 4.6-1. Voltages Seen by the ADC

Current Range (mA)	Termination Resistor	ADC Voltage Input (V_{ADC})
0 to 25	250	0 to 6.25 VDC
0 to 25	500	Not Recommended
0 to 20	250	0 to 5 VDC
0 to 20	500	0 to 10 VDC
4 to 20	250	1 to 5 VDC
4 to 20	500	2 to 10 VDC
5 to 25	250	1.25 to 6.25 VDC
5 to 25	500	Not Recommended

Use the formula: $I = \frac{V_{ADC}}{R_{Termination}}$

to convert the ADC readings to the actual current signal.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

****
* CAUTION *
****

THE MAJORITY OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS COULD BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

****
* CAUTION *
****

DO NOT INSTALL OR REMOVE BOARD WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 JUMPER INSTALLATIONS

Figure 5.3-1 on page 5-3 identifies the location of configuration jumpers and calibration potentiometers for the VMIVME-3801. Jumpers E7 through E15 are address jumpers which must be set to the desired base address of the board as described in Section 5.3.1. Jumper E16 controls the VMEbus access mode; supervisory, nonprivileged or both. This function is documented in Section 5.3.2. The remaining jumpers must be set according to Section 5.3.3 to configure the board's analog inputs.

5.3.1 Board Address

The VMIVME-3801 occupies 128 contiguous bytes of short I/O address space (see Section 4 for register details). The base address is controlled by jumpers E7 through E14 according to Table 5.3.1-1. Each installed jumper corresponds to a binary 0, while each jumper omitted corresponds to a binary 1. For base address calculation, note that address bits A0 through A6 are assumed to be zero. The factory default address is at short I/O $0000 (all jumpers installed).

Table 5.3.1-1. Address Selection Jumpers

SHORT I/O ADDRESS BIT	JUMPER # (INSTALLED=0, REMOVED=1)
A15	E15*
A14	E14*
A13	E13*
A12	E12*
A11	E11*
A10	E10*
A9	E9*
A8	E8*
A7	E7*

* Installed for factory default address of $0000.

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To change the address, first determine the new address in hexadecimal (note that the address must be an even multiple of 128 decimal, or $80). Convert the address to binary and assign the address bits A0 through A15 to the binary address starting from the LSB. Then check Table 5.3.1-1. All clear bits have a jumper installed on the corresponding address bit jumper, and all set bits have a jumper removed.

For example, assume a target address of $3A00 is desired. In binary, that number is %0011 1010 0000 0000. Assigning address bits to show that only bits A13, A12, A11, and A9 are set. Checking Table 5.3.1-1, all jumpers should be installed except for jumpers E13, E12, E11, and E9 for the target address or (desired) address.

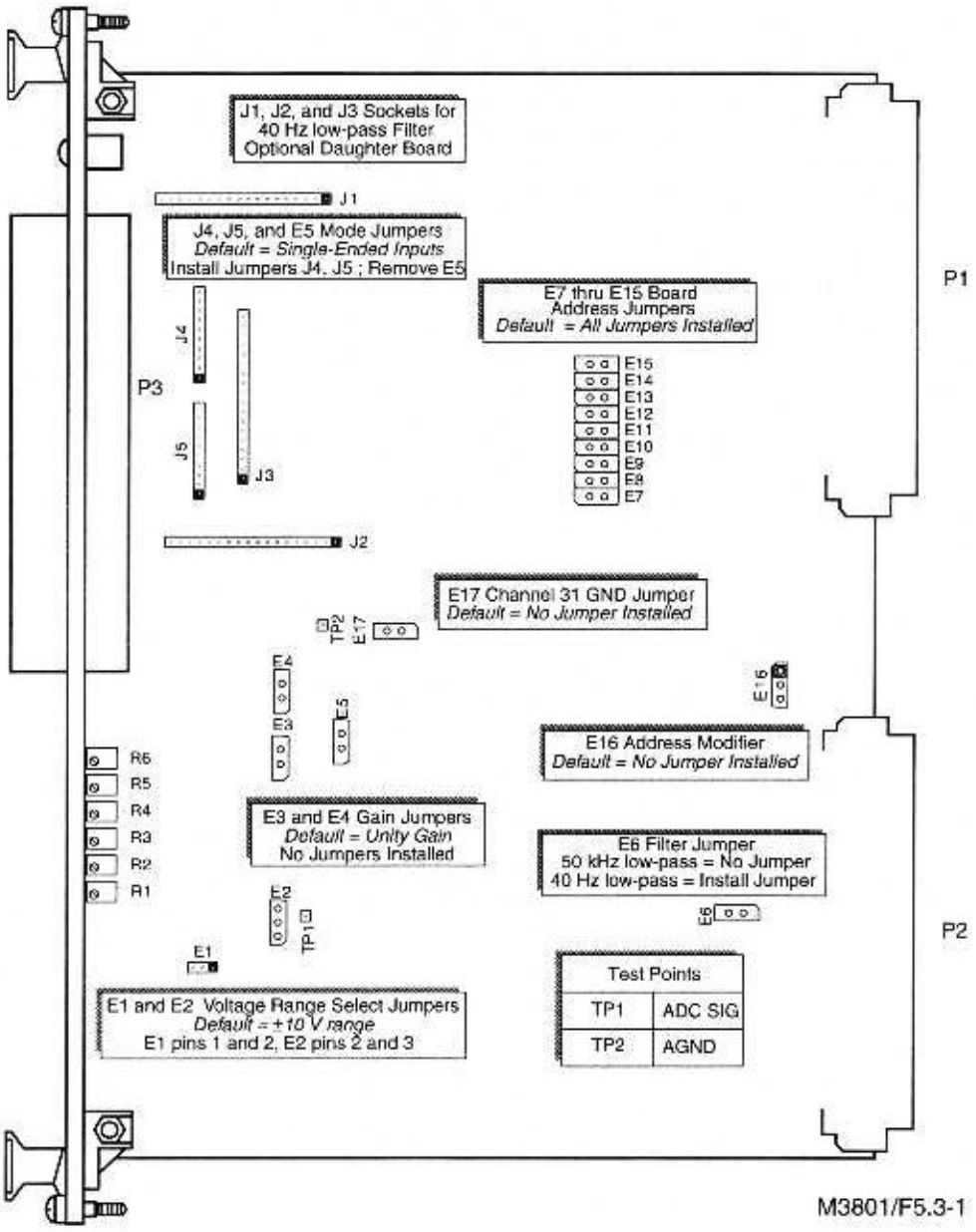

Figure 5.3-1. VMIVME-3801 Configuration Jumper Locations

5.3.2 Address Modifier

Jumper E16 determines whether the VMIVME-3801 responds to supervisory, nonprivileged, or both accesses according to Table 5.3.2-1. Default is nonprivileged.

Table 5.3.2-1. Address Modifier Jumper Settings

SHORT I/O ADDRESSING MODE	JUMPER E16 SETTING
SUPERVISORY	1-2
*NONPRIVILEGED	2-3
BOTH	NO JUMPER

*Denotes factory default. M3801/T5.3.2-1

5.3.3 Input Configuration

Three jumpers (J4, J5, and E5) are used to configure the VMIVME-3801 for single-ended or differential inputs. Two jumpers (E1 and E2) control the input voltage range, and two jumpers (E3 and E4) control the amount of gain. The jumpers are shown in Table 5.3.3-1. The factory default configuration is single-ended, ±10 V range, and unity gain.

Table 5.3.3-1. Input Configuration Jumpers

INPUT CONFIGURATION OPTION		JUMPER CONFIGURATION
MODE	SINGLE-ENDED INPUTS*	INSTALL JUMPERS J4†, J5†; REMOVE E5
	DIFFERENTIAL INPUTS	REMOVE JUMPERS J4, J5; INSTALL E5
RANGE	±10 V RANGE*	INSTALL JUMPERS E1 PINS 1 AND 2; E2 PINS 2 AND 3
	±5 V RANGE	INSTALL JUMPERS E1 PINS 1AND 2; E2 PINS 1 AND 2
	0-10 V RANGE	INSTALL JUMPERS E1 PINS 2 AND 3; E2 PINS 1AND 2
GAIN	UNITY GAIN*	REMOVE JUMPERS E4 AND E3
	X10 GAIN	REMOVE JUMPER E4; INSTALL JUMPER E3
	X100 GAIN	INSTALL JUMPER E4; REMOVE JUMPER E3
FILTER	50 kHz LOW PASS FILTER** (NO DAUGHTER BOARD)	REMOVE JUMPER E6
	40 Hz LOW-PASS FILTER** (DAUGHTER BOARD INSTALLED)	INSTALL JUMPER E6

* Indicates factory default.
**Depending on option order.
† Note that J4 and J5 must be jumpered with a "zero ohm" SIP pack (included).

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Depending on the ordering option, the board comes factory configured for either 50 kHz input filters or 40 Hz input filters. If the 40 Hz input filter option is ordered, a daughter board is factory installed into sockets J1, J2, and J3. If the 50 kHz input filter option is ordered, there is no daughter board installed and sockets J1, J2, and J3 remain empty. Jumper E17 is used to connect channel 31 to ground, this is the only method for connecting channel 31 to ground in the Single-Ended mode. The default for jumper E17 is no jumper installed.

For the -2BC and -3BC current input options, configure the VMIVME-3801 as follows:

- Single-ended 31 channels
- 0 to 10 VDC range
- Unity gain

5.4 ANALOG INPUT CONNECTOR DESCRIPTION

The 16 differential or 31 single-ended analog input connections to the VMIVME-3801 board are made using the front panel 32-pin DIN connector labelled P3. See Figure 5.4.1-1 and Table 5.4.1-1 for connector pin and signal assignments. The connector is supplied with integral latches. To remove connector depress both latches simultaneously, while gently pulling connector from socket. Install connector by aligning keying and pressing the connector into place.

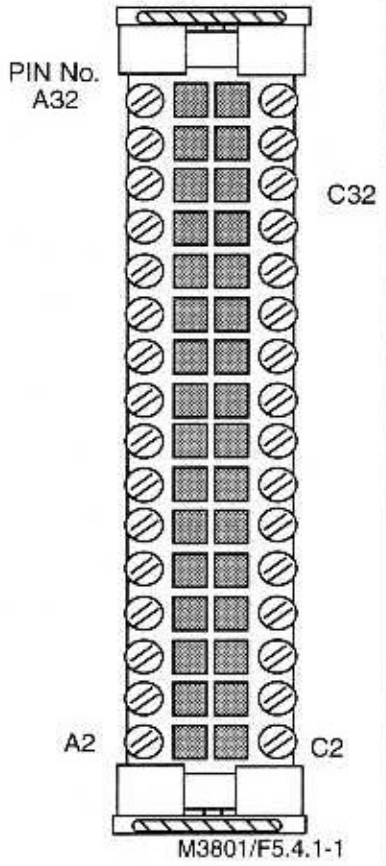
5.4.1 32-Pin DIN Connector: Connector Specification

a. Wire should be 14-22 AWG
b. Insulation stripping length: .315 in. ±.20 in./8 mm ±0.5 mm
c. The binding screw terminals are best suited for a .138 in. x.20 in./3.5 mm x 0.5 mm common flat-blade screwdriver
d. Recommended screw tightening torque: 5.22 lb/in. /0.6 mN
e. Contact resistance: ≤10 mΩ
f. Maximum current rating (+68 °F/+20 °C) 15 A
g. Operating Voltage: UL Rating 300 V

NOTE:

DUE TO CHASSIS VIBRATION VMIC RECOMMENDS PERIODIC CHECKS OF SCREW TORQUE.

Table 5.4.1-1. P3 Analog Connector Pinout



SINGLE-ENDED SIGNAL			DIFFERENTIAL SIGNAL		
PIN No.	ROW C	ROW A	PIN No.	ROW C	ROW A
32	CH31	CH30	32	CH15 LO	CH15 HI
30	CH29	CH28	30	CH14 LO	CH14 HI
28	CH27	CH26	28	CH13 LO	CH13 HI
26	CH25	CH24	26	CH12 LO	CH12 HI
24	CH23	CH22	24	CH11 LO	CH11 HI
22	CH21	CH20	22	CH10 LO	CH10 HI
20	CH19	CH18	20	CH9 LO	CH9 HI
18	CH17	CH16	18	CH8 LO	CH8 HI
16	CH15	CH14	16	CH7 LO	CH7 HI
14	CH13	CH12	14	CH6LO	CH6 HI
12	CH11	CH10	12	CH5 LO	CH5 HI
10	CH9	CH8	10	CH4LO	CH4 HI
8	CH7	CH6	8	CH3 LO	CH3 HI
6	CH5	CH4	6	CH2LO	CH2 HI
4	CH3	CH2	4	CH1 LO	CH1 HI
2	CH1	CH0	2	CH0 LO	CH0 HI

Figure 5.4.1-1. P3 Connector

M3801/T5.4.1-1

5.5 CALIBRATION PROCEDURES

In order to obtain the specified accuracy for analog measurements, the VMIVME-3801 must be calibrated for the range and input topology desired. For greatest possible accuracy, VMIC recommends calibrating the board after it has been installed in its target chassis with power applied for at least thirty minutes. Always perform the Instrumentation Amp Offset and BIT Calibration procedures first. Then select the offset and gain calibration procedure for the input topology desired. See Figure 5.3-1 on page 5-3 for the locations of test points and user-adjustable potentiometers used in the calibration of the board.

5.5.1 Equipment Required

a. 5-digit Digital Voltmeter (DVM)
b. Precision Voltage Reference

5.5.2 Instrumentation Amp Offset and BIT Voltage Calibration

NOTE:

THIS PROCEDURE MUST BE PERFORMED FIRST.

a. Configure the board for differential unipolar 0 to 10 V range:
Install jumpers E1 pins 2 and 3, E2 pins 1 and 2
Remove jumpers E3, E4, E5, J4, and J5

b. If this is the first run through this procedure, center potentiometer R5.

c. Attach the DVM positive lead to ADC input at TP1; attach the negative lead to analog ground at TP2.

d. Stop scanning on channel 0 and monitor the ADC output (a small program will be needed to do this).

e. Short channel 0's HI and LO inputs together (Row A pin 2 and Row C pin 2).

f. Install jumper E4 (sets the gain to x100).

g. Adjust the instrument amp's input offset potentiometer R6 until DVM reads as near 0.000 mVDC as possible (acceptable range is 0.0 mV to 0.3 mV).

h. Remove jumper E4 (sets the gain to x1 (unity gain)).

i. Adjust the instrument amp's output offset potentiometer R5 until DVM reads as near 0.000 VDC as possible (acceptable range is 0.0 mV to 0.3 mV).

j. Repeat steps f through i until there is no change in the output (acceptable range is 0.0 mV to 0.3 mV).

NOW CALIBRATE THE BIT REFERENCE VOLTAGE.

k. Set the gain of the board to x1 by removing the jumper from E4.
Apply the 4.980 VDC BIT voltage to channel 0 by writing the appropriate value to the mode bits in the Control/Status Register of the board.

l. Adjust potentiometer R4 until the DVM reads the correct value.

Leave the DVM connected to the board and skip to the calibration procedure for the input topology and range desired.

5.5.3 Unipolar 0-10 V Offset and Gain Calibration

NOTE:

RUN THIS CALIBRATION PROCEDURE ONLY IF THE BOARD IS TO REMAIN IN THIS CONFIGURATION WHEN INSTALLED IN THE SYSTEM.

a. Configure the board for unipolar 0-10 V inputs by installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2.

b. Configure the board for the gain to use:

E4	E3	GAIN
off	off	x1
off	on	x10
on	off	x100
on	on	x109 (**DO NOT USE**)

c. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0 (positive (+) lead to input HI, and negative (-) lead to input LO).

NOTE:

FOLLOW THE STEPS IN SECTION 5.5.3 FOR THE -2BC AND -3BC CURRENT INPUT OPTIONS. REMOVE THE -0158 TERMINATION BOARD DURING CALIBRATION. REINSTALL WHEN CALIBRATION IS COMPLETE. THE BOARD SHOULD BE IN THE SINGLE-ENDED, 0 TO 10 VDC RANGE, WITH A GAIN OF X1.

d. Input a voltage (depending on the gain) that is 1/2 LSB above ground.

GAIN	Vin
x1	1.22 mVDC
x10	122.1 µVDC
x100	12.21 µVDC

e. While monitoring the ADC output of channel 0, adjust the unipolar offset potentiometer R3 until the display is fluctuating between $000 and $001.

f. Input a voltage (depending on the gain) that is 11/2 LSB below the maximum input.

GAIN	Vin
x1	9.996338 VDC
x10	0.999634 VDC
x100	0.099963 VDC

g. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display fluctuates between $FFE and $FFF.

h. Repeat steps d through g at least once or until no adjustment is necessary.

This concludes the calibration of the VMIVME-3801.

5.5.4 Bipolar ±5 V Differential Inputs Offset and Gain Calibration

NOTE:

RUN THIS CALIBRATION PROCEDURE ONLY IF THE BOARD IS TO REMAIN IN THIS CONFIGURATION WHEN INSTALLED IN THE SYSTEM.

a. Configure the board for bipolar ±5 V inputs by installing a jumper on E1 pins 1 and 2, E2 pins 1 and 2.

b. Configure the board for the desired gain:

E4	E3	GAIN
off	off	x1
off	on	x10
on	off	x100
on	on	x109 (**DO NOT USE**)

c. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0 (positive (+) lead to input HI and negative (-) lead to input LO).

d. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

GAIN	Vin
x1	-4.998779 VDC
x10	-0.499878 VDC
x100	-0.049988 VDC

e. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display fluctuates between $000 and $001.

f. Input a voltage (depending on the gain) that is 11/2 LSB below the maximum input.

GAIN	Vin
x1	4.996338 VDC
x10	0.499634 VDC
x100	0.049963 VDC

g. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.

h. Repeat steps d through g at least once or until no adjustment is necessary.

This concludes the calibration of the VMIVME-3801.

5.5.5 Bipolar ±10 V Differential Inputs Offset and Gain Calibration

NOTE:

RUN THIS CALIBRATION PROCEDURE ONLY IF THE BOARD IS TO REMAIN IN THIS CONFIGURATION WHEN INSTALLED IN THE SYSTEM.

a. Configure the board for bipolar ±10 V inputs by installing a jumper on E1 pins 1 and 2, E2 pins 2 and 3.

b. Configure the board for the desired gain:

E4	E3	GAIN
off	off	x1
off	on	x10
on	off	x100
on	on	x109 (**DO NOT USE**)

c. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0 (positive (+) lead to input HI and negative (-) lead to input LO).

d. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

GAIN	Vin
x1	-9.997559 VDC
x10	-0.999756 VDC
x100	-0.099976 VDC

e. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display is fluctuating between $000 and $001.

f. Input a voltage (depending on the gain) that is 11/2 LSB below the maximum input.

GAIN	Vin
x1	9.992676 VDC
x10	0.999268 VDC
x100	0.099927 VDC

g. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.

h. Repeat steps d through g at least once or until no adjustment is necessary.

This concludes the calibration of the VMIVME-3801.

5.5.6 Unipolar 0 - 10 V Single-Ended Inputs Offset and Gain Calibration

NOTE:

RUN THIS CALIBRATION PROCEDURE ONLY IF THE BOARD IS TO REMAIN IN THIS CONFIGURATION WHEN INSTALLED IN THE SYSTEM.

a. Configure the board for unipolar 0-10 V single-ended inputs by installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2, J4, and J5 remove E5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)

b. Configure the board for the desired gain:

E4	E3	GAIN
off	off	x1
off	on	x10
on	off	x100
on	on	x109 (**DO NOT USE**)

c. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)

d. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector C32 with E17 installed).

e. Input a voltage (depending on the gain) that is 1/2 LSB above ground.

GAIN	Vin
x1	1.221 mVDC
x10	122.1 µVDC
x100	12.21 µVDC

f. While monitoring the ADC output of channel 0, adjust the unipolar offset potentiometer R3 until the display is fluctuating between $000 and $001.

g. Input a voltage (depending on the gain) that is 11/2 LSB below the maximum input.

GAIN	Vin
x1	9.996338 VDC
x10	0.999634 VDC
x100	0.099963 VDC

h. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.

i. Repeat steps e through h at least once or until no adjustments are necessary.

This concludes the calibration of the VMIVME-3801.

5.5.7 Bipolar ±5 V Single-Ended Inputs Offset and Gain Calibration

NOTE:

RUN THIS CALIBRATION PROCEDURE ONLY IF THE BOARD IS TO REMAIN IN THIS CONFIGURATION WHEN INSTALLED IN THE SYSTEM.

a. Configure the board for unipolar ±5 V single-ended inputs by installing a jumper on E1 pins 1 and 2, E2 pins 1 and 2, J4, and J5 remove E5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)

b. Configure the board for the desired gain:

E4	E3	GAIN
off	off	x1
off	on	x10
on	off	x100
on	on	x109 (**DO NOT USE**)

c. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)

d. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector C32 with E17 installed).

e. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

GAIN	Vin
x1	-4.998779 VDC
x10	-0.499878 VDC
x100	-0.049988 VDC

f. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display is fluctuating between $000 and $001.

g. Input a voltage (depending on the gain) that is 11/2 LSB below the maximum input.

GAIN	Vin
x1	4.996338 VDC
x10	0.499634 VDC
x100	0.049963 VDC

h. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.

i. Repeat steps e through h at least once or until no adjustments are necessary.

This concludes the calibration of the VMIVME-3801.

5.5.8 Bipolar ±10 V Single-Ended Inputs Offset and Gain Calibration

NOTE:

RUN THIS CALIBRATION PROCEDURE ONLY IF THE BOARD IS TO REMAIN IN THIS CONFIGURATION WHEN INSTALLED IN THE SYSTEM.

a. Configure the board for unipolar ±10 V single-ended inputs by installing a jumper on E1 pins 1 and 2, E2 pins 2 and 3, J4, and J5 remove E5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)

b. Configure the board for the desired gain:

E4	E3	GAIN
off	off	x1
off	on	x10
on	off	x100
on	on	x109 (**DO NOT USE**)

c. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)

d. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector C32 with E17 installed).

e. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

GAIN	Vin
x1	-9.997559 VDC
x10	-0.999756 VDC
x100	-0.099976 VDC

f. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display is fluctuating between $000 and $001.

g. Input a voltage (depending on the gain) that is 11/2 LSB below the maximum input.

GAIN	Vin
x1	9.992676 VDC
x10	0.999268 VDC
x100	0.099927 VDC

h. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.

i. Repeat steps e through h at least once or until no adjustments are necessary.

This concludes the calibration of the VMIVME-3801.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

6.2 MAINTENANCE PRINTS

User level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC