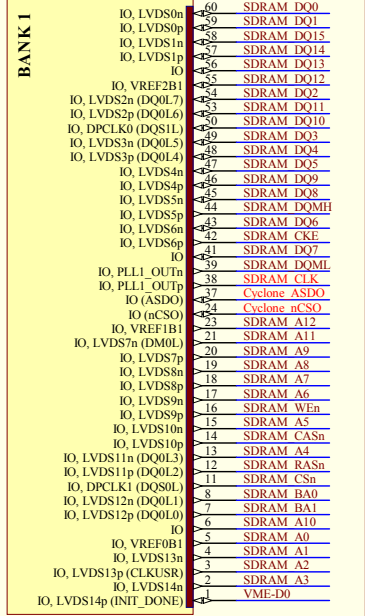
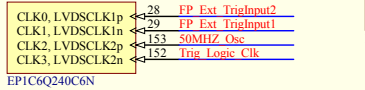


CY1A

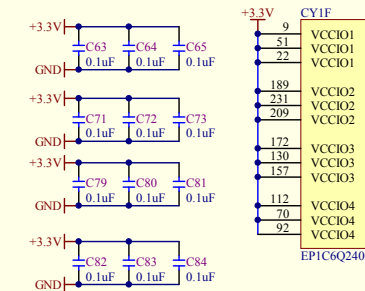
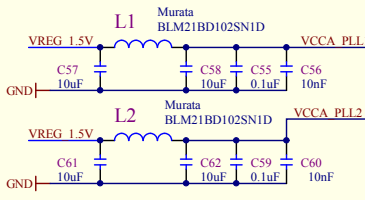


EPIC6Q240C6N

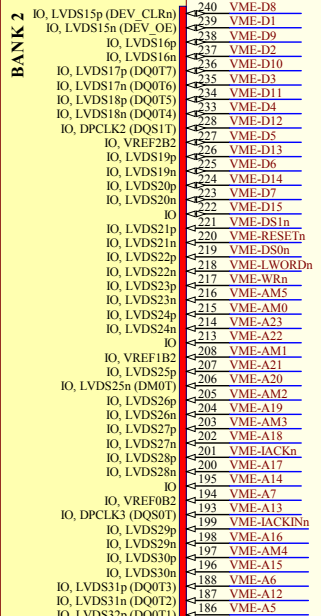
CY1H



EPIC6Q240C6N

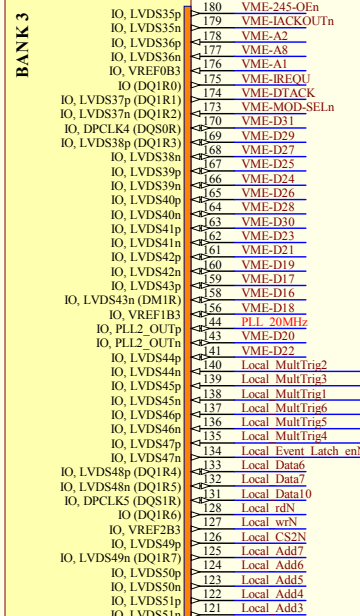


CY1B

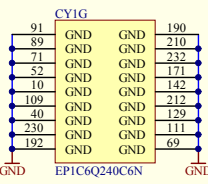


EPIC6Q240C6N

CY1C

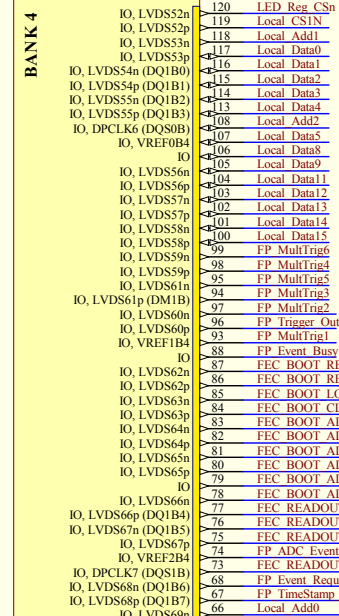


EPIC6Q240C6N

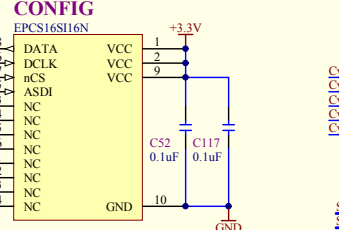


EPIC6Q240C6N

CY1D

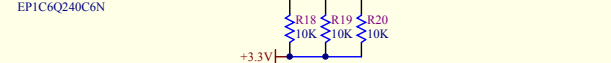
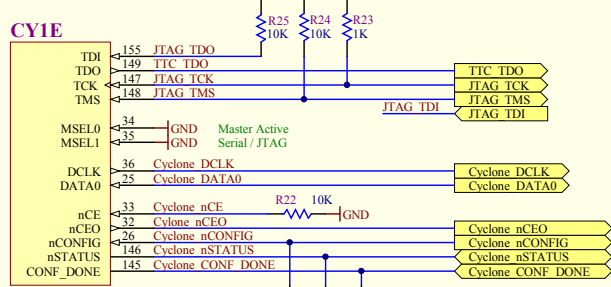


EPIC6Q240C6N

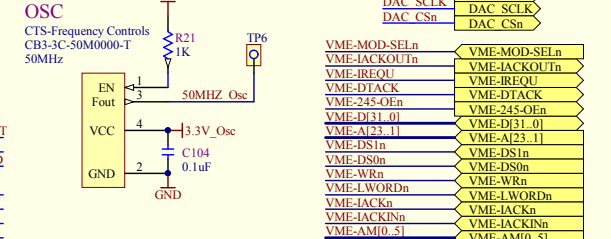


PLL Clock Driver 1-5

CY1E



OSCI

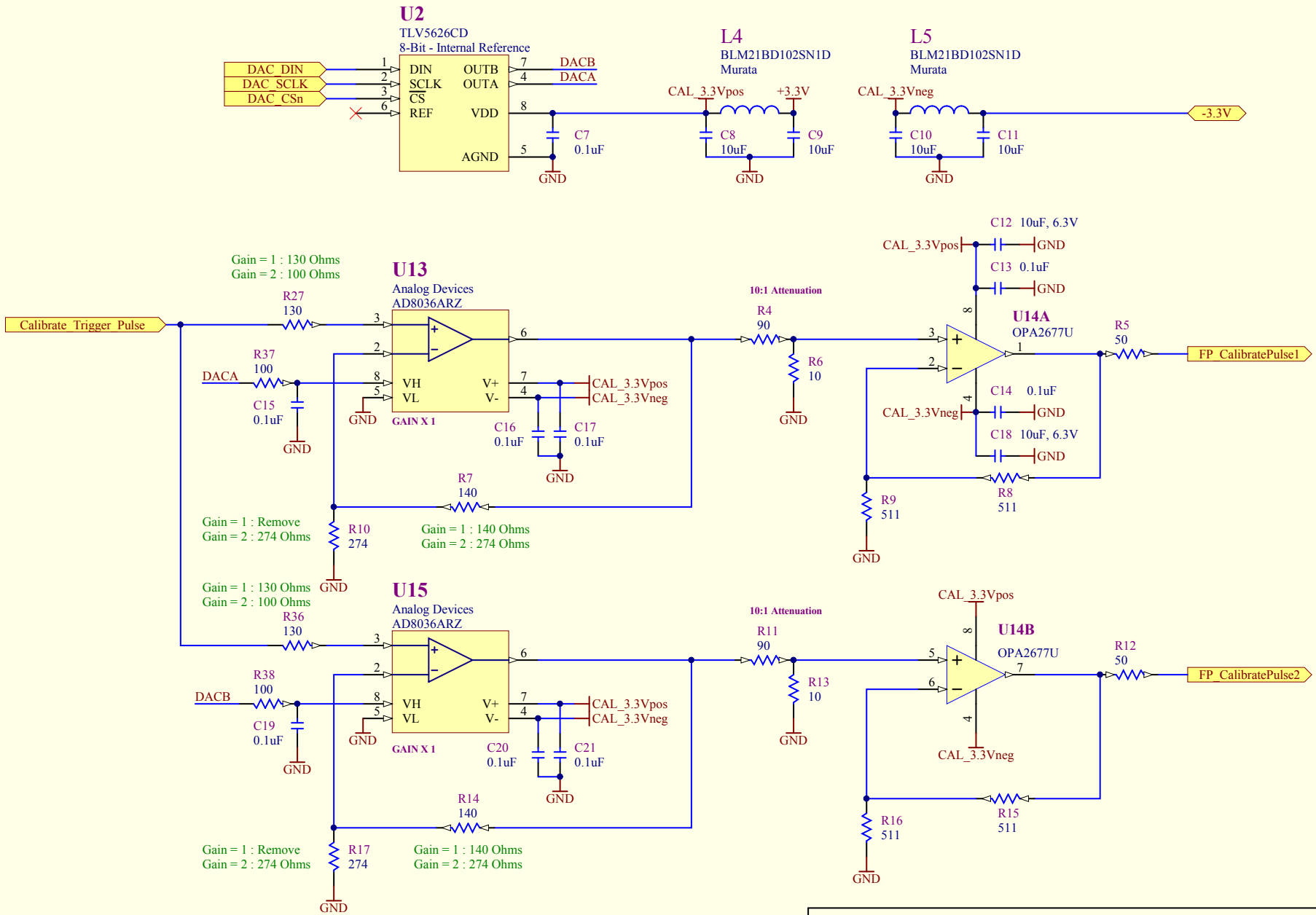


ACT\_SER

**ALPHA TTC - Trigger Logic**

Revision: 0	Drawing #: 0	TRUMF 4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
Sheet # 1 of 12	Size: B	
Drawn by: D.Bishop	Date: 11/05/2009	

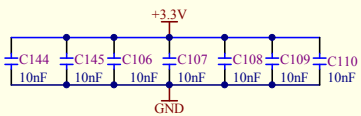
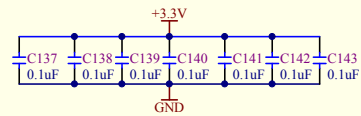
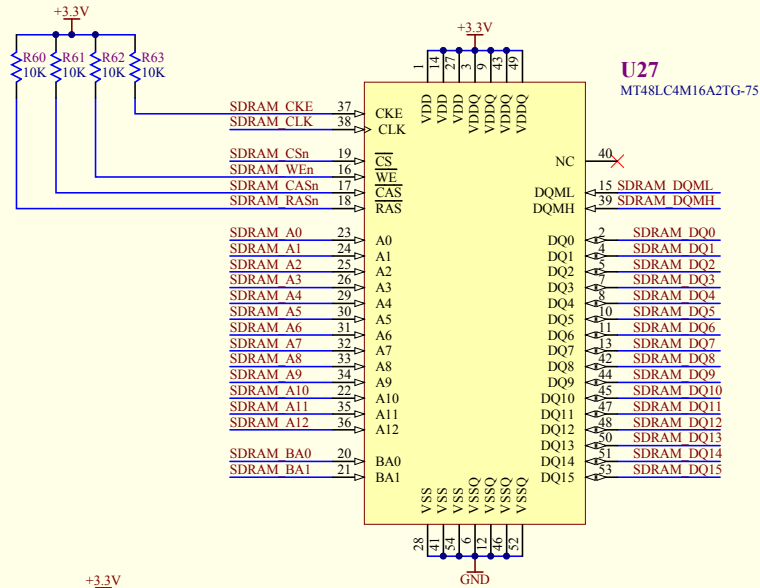
File: G:\AH\WALPHA\TTC\AlphaTTC - Trigger Logic.SCHDOC 3:34:42 PM




ALPHA TTC - Calibrate Pulse			
Revision	Drawing #:		<b>TRIUMF</b> 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
<b>0</b>	Sheet #: 2	of 12	
	Drawn by: D.Bishop	Date: 11/05/2009	
File: G:\AHW\ALPHA\TTC\Altium\ALPHA TTC - Calibrate Pulse.SCHDOC			



SDRAM DQ[0..15]	SDRAM DQ[0..15]
SDRAM A[0..12]	SDRAM A[0..12]
SDRAM BA[0..1]	SDRAM BA[0..1]
SDRAM DQMH	SDRAM DQMH
SDRAM DQML	SDRAM DQML
SDRAM WEn	SDRAM WEn
SDRAM CASn	SDRAM CASn
SDRAM RASn	SDRAM RASn
SDRAM CSn	SDRAM CSn
SDRAM CKE	SDRAM CKE
SDRAM CLK	SDRAM CLK



**ALPHA TTC - SDRAM**

Revision <b>0</b>	Drawing #:	<b>TRIUMF</b> 4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3		
	Sheet # 3 of 12			Size: A
	Drawn by: D.Bishop			Date: 11/05/2009
File: G:\AHW\ALPHA\TTC\Altium\ALPHA TTC - SDRAM.SCHDOC				
			3:34:43 PM	

**UIA**

**BANK 1**

IO, LVDS0n	60	Mictor10
IO, LVDS0p	59	Mictor11
IO, LVDS1n	58	Mictor12
IO, LVDS1p	57	Mictor13
IO, LVDS1n	56	Local wrN
IO, LVDS1p	55	Local CSn
IO, VREF2B1	54	Trigger IN44
IO, LVDS2n (DQ0L7)	53	Trigger IN43
IO, LVDS2p (DQ0L6)	50	Trigger IN48
IO, DPCLK0 (DQS1L)	49	Trigger IN21
IO, LVDS3n (DQ0L5)	48	Trigger IN34
IO, LVDS3p (DQ0L4)	47	Trigger IN38
IO, LVDS4n	46	Trigger IN35
IO, LVDS4p	45	Trigger IN37
IO, LVDS5n	44	Trigger IN40
IO, LVDS5p	43	Trigger IN39
IO, LVDS6n	42	Trigger IN42
IO, LVDS6p	41	Trigger IN2
IO	39	Trigger IN28
IO, PLL1_OUTn	38	Trigger IN26
IO, PLL1_OUTp	37	Trigger IN24
IO (ASD0)	24	Trigger IN22
IO (nCS0)	23	Trigger IN23
IO, VREF1B1	21	Trigger IN27
IO, LVDS7n (DM0L)	20	Trigger IN25
IO, LVDS7p	19	Trigger IN18
IO, LVDS8n	18	Trigger IN19
IO, LVDS8p	17	Trigger IN29
IO, LVDS9n	16	Trigger IN2
IO, LVDS9p	15	Trigger IN3
IO, LVDS10n	14	Trigger IN6
IO, LVDS10p	13	Trigger IN12
IO, LVDS11n (DQ0L3)	12	Trigger IN16
IO, LVDS11p (DQ0L2)	11	Trigger IN5
IO, DPCLK1 (DQS1L)	8	Trigger IN10
IO, LVDS12n (DQ0L1)	7	Trigger IN8
IO, LVDS12p (DQ0L0)	6	Trigger IN7
IO, VREF0B1	5	Trigger IN9
IO, LVDS13n	4	Trigger IN11
IO, LVDS13p (CLKUSR)	3	Trigger IN13
IO, LVDS14n	2	Trigger IN14
IO, LVDS14p (INT1_DONE)	1	Trigger IN15

**UIB**

**BANK 2**

IO, LVDS15p (DEV_CLRn)	240	Trigger IN30
IO, LVDS15n (DEV_OE)	239	Trigger IN31
IO, LVDS16p	238	Trigger IN46
IO, LVDS16n	237	Trigger IN47
IO, LVDS17p (DQ0I7)	236	Trigger IN68
IO, LVDS17n (DQ0I6)	235	Trigger IN62
IO, LVDS17n (DQ0I6)	234	Trigger IN63
IO, LVDS18p (DQ0I5)	233	Trigger IN60
IO, LVDS18n (DQ0I4)	228	Trigger IN64
IO, DPCLK2 (DQS1R)	227	Trigger IN59
IO, VREF2B3	226	Trigger IN57
IO, LVDS19p	225	Trigger IN58
IO, LVDS19n	224	Trigger IN55
IO, LVDS20p	223	Trigger IN56
IO, LVDS20n	222	Trigger IN54
IO	221	Trigger IN53
IO, LVDS21p	220	Trigger IN51
IO, LVDS21n	219	Trigger IN52
IO, LVDS22p	218	Trigger IN50
IO, LVDS22n	217	Trigger IN49
IO, LVDS23p	216	Trigger IN36
IO, LVDS23n	215	Trigger IN33
IO, VREF1B3	214	Trigger IN20
IO, LVDS24p	213	Trigger IN17
IO, LVDS24n	208	Trigger IN4
IO, VREF1B2	207	Trigger IN1
IO, LVDS25p	206	Trigger IN78
IO, LVDS25n (DM0I)	205	Trigger IN79
IO, LVDS26p	204	Trigger IN94
IO, LVDS26n	203	Trigger IN95
IO, LVDS27p	202	Trigger IN10
IO, LVDS27n	201	Trigger IN11
IO, LVDS28p	200	Trigger IN28
IO, LVDS28n	195	Trigger IN22
IO	194	Trigger IN21
IO, VREF0B2	193	Trigger IN23
IO, DPCLK3 (DQS0I)	199	Trigger IN126
IO, LVDS29p	198	Trigger IN127
IO, LVDS29n	197	Trigger IN124
IO, LVDS30p	196	Trigger IN125
IO, LVDS30n	188	Trigger IN18
IO, LVDS31p (DQ0I3)	187	Trigger IN20
IO, LVDS31n (DQ0I2)	186	Trigger IN19
IO, LVDS32p (DQ0I1)	185	Trigger IN17
IO, LVDS32n (DQ0I0)	184	Trigger IN14
IO, LVDS33p	183	Trigger IN16
IO, LVDS33n	182	Trigger IN15
IO, LVDS34p	181	Trigger IN13
IO, LVDS34n		

**UIC**

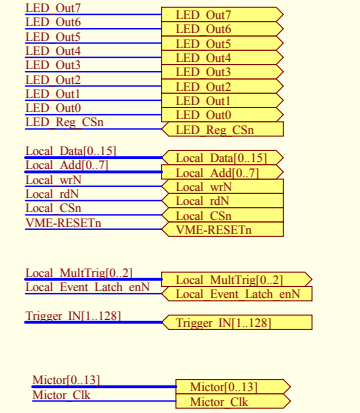
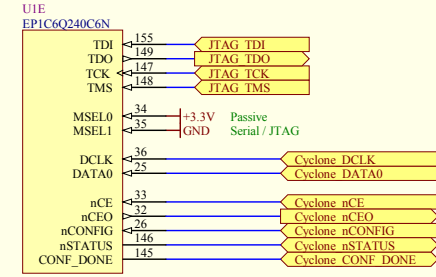
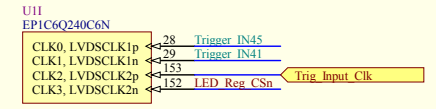
**BANK 3**

IO, LVDS35p	180	Trigger IN100
IO, LVDS35n	179	Trigger IN97
IO, LVDS36p	178	Trigger IN84
IO, LVDS36n	177	Trigger IN81
IO, VREF0B3	176	Trigger IN68
IO, VREF0B3	175	Trigger IN65
IO (DQI1R5)	174	Trigger IN70
IO, LVDS37p (DQI1R1)	173	Trigger IN66
IO, LVDS37n (DQI1R2)	172	Trigger IN69
IO, DPCLK4 (DQS0R)	170	Trigger IN69
IO, LVDS38p (DQI1R3)	169	Trigger IN72
IO, LVDS38n	168	Trigger IN71
IO, LVDS39p	167	Trigger IN73
IO, LVDS39n	166	Trigger IN75
IO, LVDS40p	165	Trigger IN77
IO, LVDS40n	164	Trigger IN74
IO, LVDS41p	163	Trigger IN76
IO, LVDS41n	162	Trigger IN80
IO, LVDS42p	161	Trigger IN99
IO, LVDS42n	160	Trigger IN98
IO, LVDS43p	159	Trigger IN102
IO, LVDS43n	158	Trigger IN101
IO, LVDS43n (DM1R)	156	Trigger IN103
IO, VREF1B3	144	Trigger IN104
IO, PLL2_OUTp	143	Trigger IN105
IO, PLL2_OUTn	141	Trigger IN107
IO, LVDS44p	140	Trigger IN109
IO, LVDS44n	139	Trigger IN106
IO, LVDS45p	138	Trigger IN108
IO, LVDS45n	137	Trigger IN112
IO, LVDS46p	136	Trigger IN83
IO, LVDS46n	135	Trigger IN82
IO, LVDS47p	134	Trigger IN89
IO, LVDS47n	133	Trigger IN91
IO, LVDS48p (DQI1R4)	132	Trigger IN93
IO, LVDS48n (DQI1R5)	131	Trigger IN90
IO, DPCLK5 (DQS1R)	128	Trigger IN67
IO (DQI1R6)	127	Trigger IN85
IO, VREF2B3	126	Trigger IN87
IO, LVDS49p	125	Trigger IN86
IO, LVDS49n (DQI1R7)	124	Trigger IN88
IO, LVDS50p	123	Trigger IN92
IO, LVDS50n	122	Trigger IN96
IO, LVDS51p	121	VME-RESE1n
IO, LVDS51n		

**UID** EPIC6Q240C6N

**BANK 4**

IO, LVDS52n	120	Local rdN
IO, LVDS52p	119	Local MultTrig1
IO, LVDS53n	118	Local MultTrig2
IO, LVDS53p	117	Local MultTrig0
IO, VREF0B4	116	LED Out7
IO, LVDS54n (DQI1B0)	115	LED Out6
IO, LVDS54p (DQI1B1)	114	LED Out5
IO, LVDS55n (DQI1B2)	113	LED Out4
IO, LVDS55p (DQI1B3)	108	LED Out3
IO, DPCLK6 (DQS0B)	107	LED Out2
IO, VREF0B4	106	LED Out1
IO	105	LED Out0
IO, LVDS56n	104	Local Event Latch_enN
IO, LVDS56p	103	Local data0
IO, LVDS57n	102	Local data1
IO, LVDS57p	101	Local data2
IO, LVDS58n	100	Local data3
IO, LVDS58p	99	Local data4
IO, LVDS59n	98	Local data5
IO, LVDS59p	95	Local data6
IO, LVDS61n	94	Local data7
IO, LVDS61p (DM1B)	94	Local data8
IO, LVDS60n	96	Local data9
IO, LVDS60p	93	Local data10
IO, VREF1B4	98	Local data11
IO	97	Local data12
IO, LVDS62n	96	Local data13
IO, LVDS62p	95	Local data14
IO, LVDS63n	84	Local data15
IO, LVDS64n	83	Local Add0
IO, LVDS64p	82	Local Add1
IO, LVDS65n	81	Local Add2
IO, LVDS65p	80	Local Add3
IO	79	Local Add4
IO	78	Local Add5
IO, LVDS66n	77	Local Add6
IO, LVDS66p (DQI1B4)	76	Local Add7
IO, LVDS67n (DQI1B5)	75	Mictor Clk
IO, LVDS67p	74	Mictor0
IO, VREF2B4	73	Mictor1
IO, DPCLK7 (DQS1B)	68	Mictor2
IO, LVDS68n (DQI1B6)	67	Mictor3
IO, LVDS68p (DQI1B7)	66	Mictor4
IO, LVDS69n	65	Mictor5
IO, LVDS69p	64	Mictor6
IO, LVDS70n	63	Mictor7
IO, LVDS70p	62	Mictor8
IO, LVDS71n	61	Mictor9
IO, LVDS71p		

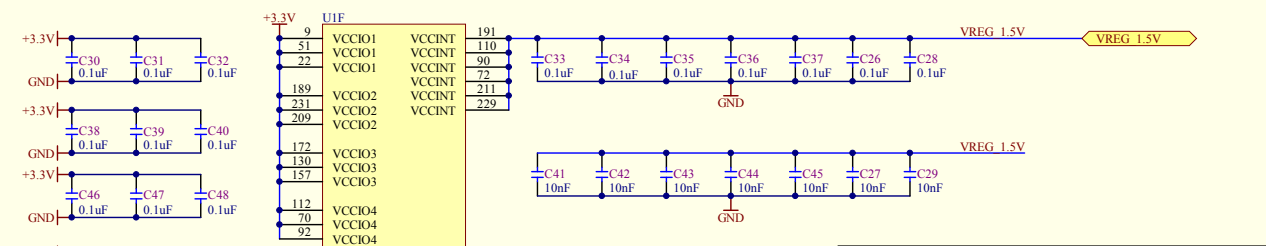
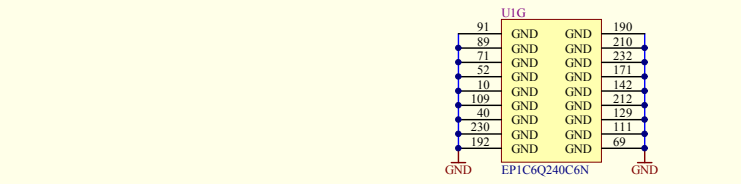
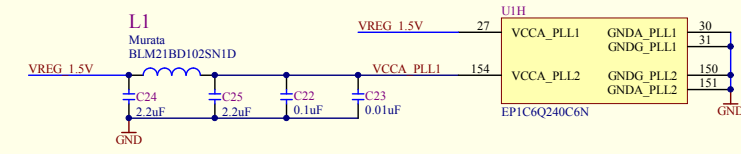


EPIC6Q240C6N

EPIC6Q240C6N

EPIC6Q240C6N

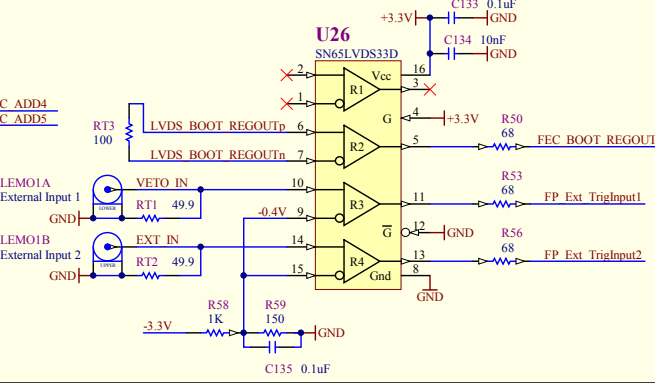
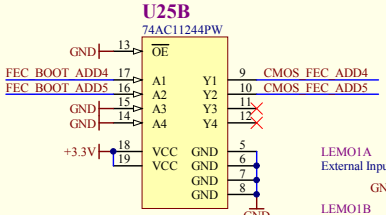
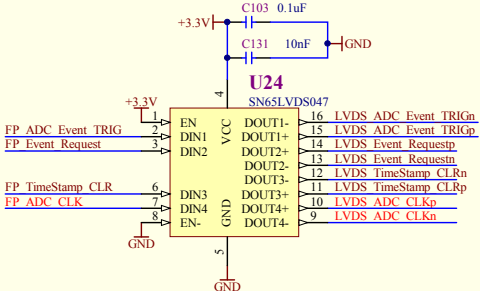
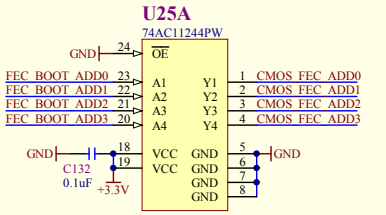
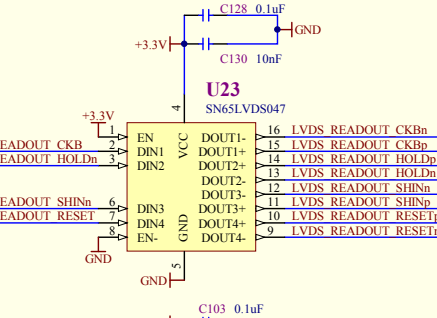
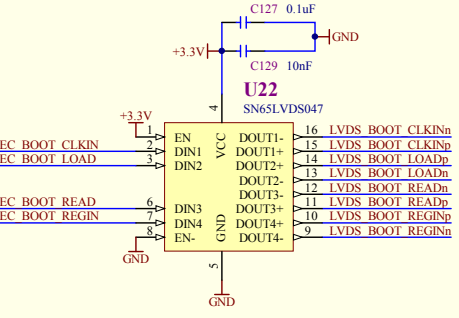
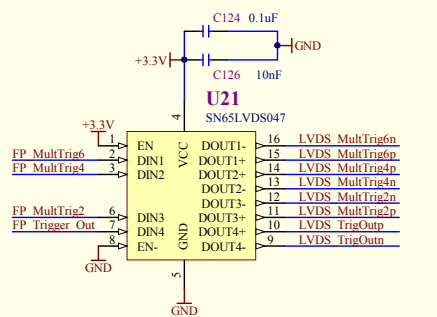
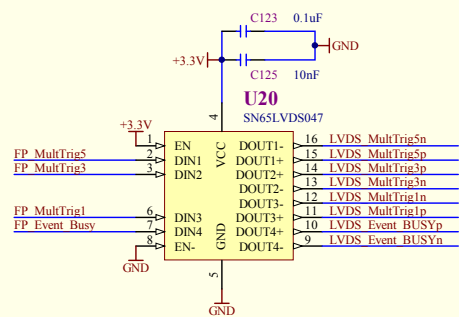
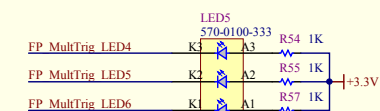
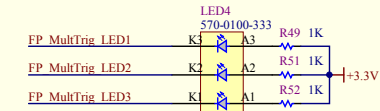
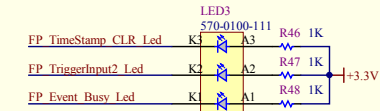
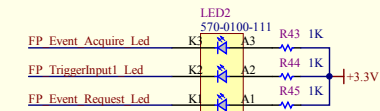
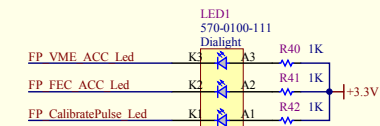
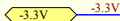
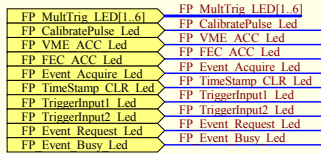
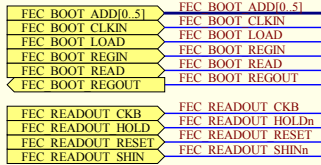
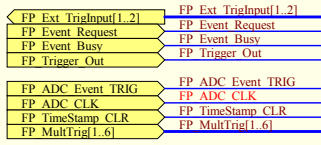
EPIC6Q240C6N



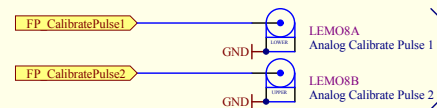
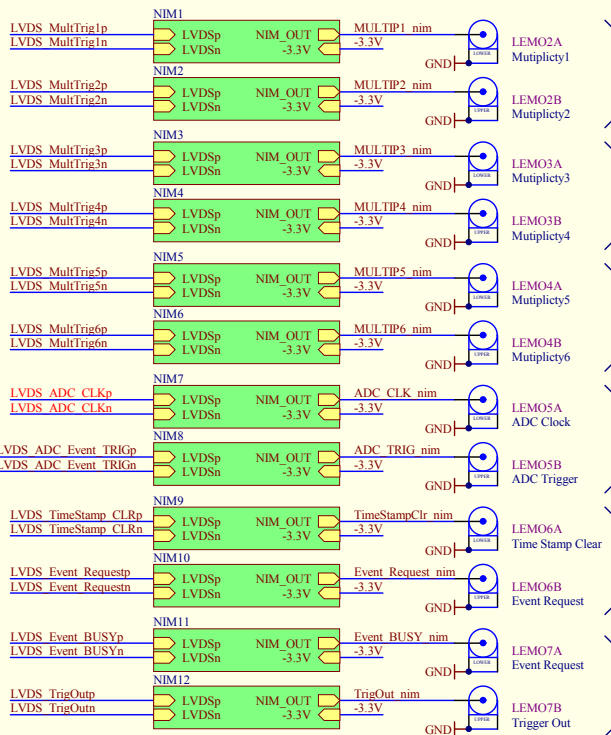
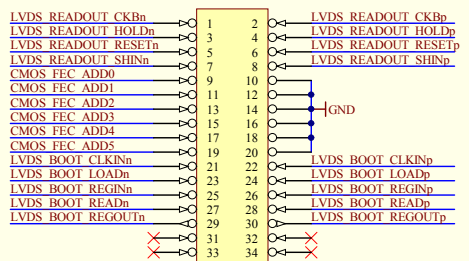
**ALPHA TTC - Trigger Input**

Revision: <b>0</b>	Drawing #: _____	TRIUMF 4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3	
Drawn by: D.Bishop	Date: 11/05/2009	Sheet #: 4 of 12 Size: B	

File: G:\AH\WALPHA\ITTC\Alpha\ALPHA TTC - Trigger Inputs.SCHDOC 3:34:43 PM



J2 FTSH-117-01-L-DV Mates with SAMTEC - FFSD Series



ALPHA TTC - Front Panel			
Revision	Drawing #:	TRIUMF	
0	Sheet # 5 of 12	4004 Westbrook Mall	
Drawn by: D.Bishop	Date: 11/05/2009	Vancouver, B.C.	
		Canada	
		V6T 2A3	
File:	G:\AHW\ALPHA\TTC\Alpha\ALPHA TTC - Front Panel.SCHDOC		
			3:34:43 PM

**CHARACTERISTICS**

T<sub>j</sub> = 25 °C unless otherwise specified.

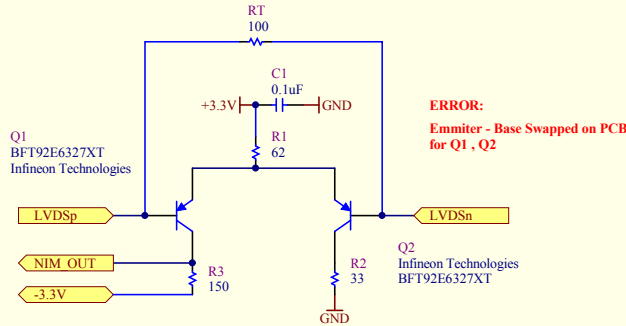
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector cut-off current	I <sub>E</sub> = 0, V <sub>CB</sub> = -10 V,	-	-	-50	nA
h <sub>FE</sub>	DC current gain	I <sub>C</sub> = -14 mA, V <sub>CE</sub> = -10 V	20	50	-	-
f <sub>T</sub>	transition frequency	I <sub>C</sub> = -14 mA, V <sub>CE</sub> = -10 V, f = 500 MHz	-	5	-	GHz
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = I <sub>B</sub> = 0, V <sub>CB</sub> = -10 V, f = 1 MHz	-	0.75	-	pF
C <sub>e</sub>	emitter capacitance	I <sub>C</sub> = I <sub>E</sub> = 0, V <sub>EB</sub> = -0.5 V, f = 1 MHz	-	0.8	-	pF
C <sub>FB</sub>	feedback capacitance	I <sub>C</sub> = -2 mA, V <sub>CE</sub> = -10 V, f = 1 MHz	-	0.7	-	pF
G <sub>UM</sub>	maximum unilateral power gain (note 1)	I <sub>C</sub> = -14 mA, V <sub>CE</sub> = -10 V, f = 500 MHz, T <sub>amb</sub> = 25 °C	-	18	-	dB
F	noise figure	I <sub>C</sub> = -5 mA, V <sub>CE</sub> = -10 V, f = 500 MHz, T <sub>amb</sub> = 25 °C	-	2.5	-	dB
V <sub>O</sub>	output voltage	note 2	-	150	-	mV

**PNP RF Transistor**  
(continued)

**Electrical Characteristics** T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
<b>OFF CHARACTERISTICS</b>					
V <sub>CE(sat)</sub>	Collector-Emitter Breakdown Voltage <sup>1</sup>	I <sub>C</sub> = 1.0 mA, I <sub>B</sub> = 0	20	-	V
V <sub>CE(sco)</sub>	Collector-Base Breakdown Voltage	I <sub>C</sub> = 10 μA, I <sub>B</sub> = 0	20	-	V
V <sub>EB(sco)</sub>	Emitter-Base Breakdown Voltage	I <sub>E</sub> = 10 μA, I <sub>C</sub> = 0	3.0	-	V
I <sub>CEO</sub>	Collector Cutoff Current	V <sub>CB</sub> = 10 V, I <sub>B</sub> = 0	-	100	nA
I <sub>EB0</sub>	Emitter Cutoff Current	V <sub>EB</sub> = 2.0 V, I <sub>C</sub> = 0	-	100	nA
<b>ON CHARACTERISTICS</b>					
h <sub>FE</sub>	DC Current Gain	I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 10 V	60	-	-
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 5.0 mA, I <sub>B</sub> = 0.5 mA	-	0.5	V
V <sub>BE(sat)</sub>	Base-Emitter On Voltage	I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 10 V	-	0.9	V
<b>SMALL SIGNAL CHARACTERISTICS</b>					
f <sub>T</sub>	Current Gain - Bandwidth Product	I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 10 V, f = 100 MHz	600	-	MHz
C <sub>cb</sub>	Collector-Base Capacitance	V <sub>CB</sub> = 10 V, I <sub>C</sub> = 0, f = 1.0 MHz	-	0.85	pF
C <sub>ce</sub>	Collector-Emitter Capacitance	V <sub>CE</sub> = 10 V, I <sub>C</sub> = 0, f = 1.0 MHz	-	0.85	pF

MPSH81 / MM8T81



Alternate - BFT92 - 5GHz - Ce 0.8pF  
 Alternate - MMBTH81 - 600 Mhz - Ccb 0.85pF  
 Alternate - MMBT3906 - 250 Mhz - Ce 10pF

**PNP General Purpose Amplifier**  
(continued)

**Electrical Characteristics** T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
<b>OFF CHARACTERISTICS</b>					
V <sub>CE(sco)</sub>	Collector-Emitter Breakdown Voltage <sup>1</sup>	I <sub>C</sub> = 1.0 mA, I <sub>B</sub> = 0	40	-	V
V <sub>CE(scb)</sub>	Collector-Base Breakdown Voltage	I <sub>C</sub> = 10 μA, I <sub>B</sub> = 0	40	-	V
V <sub>EB(sco)</sub>	Emitter-Base Breakdown Voltage	I <sub>E</sub> = 10 μA, I <sub>C</sub> = 0	5.0	-	V
I <sub>CE0</sub>	Base Cutoff Current	V <sub>CB</sub> = 30 V, V <sub>EB</sub> = 3.0 V	-	50	nA
I <sub>CEX</sub>	Collector Cutoff Current	V <sub>CB</sub> = 30 V, V <sub>EB</sub> = 3.0 V	-	50	nA
<b>ON CHARACTERISTICS</b>					
h <sub>FE</sub>	DC Current Gain <sup>2</sup>	I <sub>C</sub> = 0.1 mA, V <sub>CE</sub> = 1.0 V I <sub>C</sub> = 1.0 mA, V <sub>CE</sub> = 1.0 V I <sub>C</sub> = 10 mA, V <sub>CE</sub> = 1.0 V I <sub>C</sub> = 50 mA, V <sub>CE</sub> = 1.0 V I <sub>C</sub> = 100 mA, V <sub>CE</sub> = 1.0 V	60 80 100 60 30	300	-
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 10 mA, I <sub>B</sub> = 1.0 mA I <sub>C</sub> = 50 mA, I <sub>B</sub> = 5.0 mA	-	0.25 0.4	V
V <sub>BE(sat)</sub>	Base-Emitter Saturation Voltage	I <sub>C</sub> = 10 mA, I <sub>B</sub> = 1.0 mA I <sub>C</sub> = 50 mA, I <sub>B</sub> = 5.0 mA	0.65	0.85 0.95	V
<b>SMALL SIGNAL CHARACTERISTICS</b>					
f <sub>T</sub>	Current Gain - Bandwidth Product	I <sub>C</sub> = 10 mA, V <sub>CE</sub> = 20 V, f = 100 kHz	250	-	MHz
C <sub>out</sub>	Output Capacitance	V <sub>CB</sub> = 5.0 V, I <sub>C</sub> = 0, f = 100 kHz	-	4.5	pF
C <sub>in</sub>	Input Capacitance	V <sub>BE</sub> = 0.5 V, I <sub>C</sub> = 0, f = 100 kHz	-	10.0	pF
NF	Noise Figure	I <sub>C</sub> = 100 μA, V <sub>CE</sub> = 5.0 V, R <sub>g</sub> = 1.0kΩ, f = 10 Hz to 15.7 kHz	-	4.0	dB

2N3906 / MM8T3906 / PZT3906

**Cyclone - LVDS**

Output Offset Voltage

V<sub>os</sub> Max - 1.375  
 V<sub>os</sub> Typ - 1.25  
 V<sub>os</sub> Min - 1.125

Diff Output Voltage

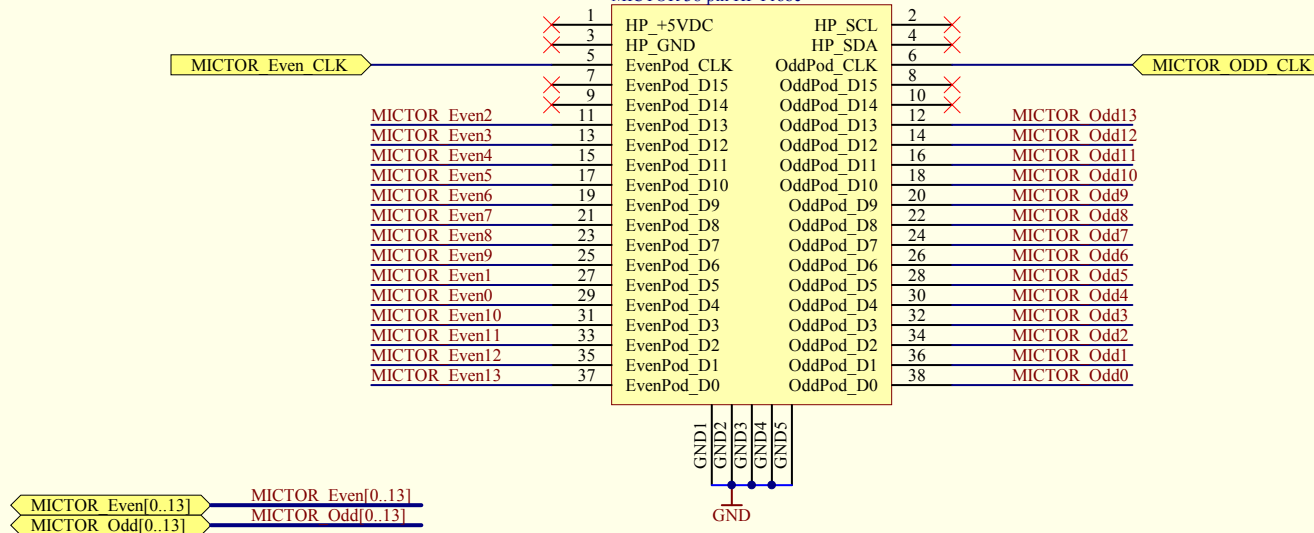
V<sub>od</sub> Min - 250mv  
 V<sub>od</sub> Max - 600mv

**ALPHA TTC - LVDS to NIM Converter**

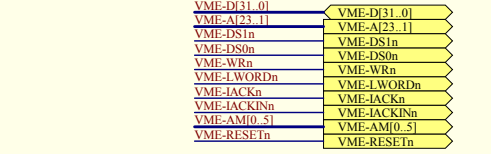
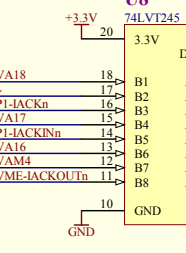
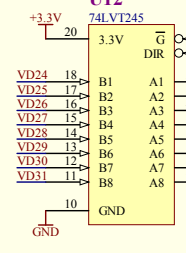
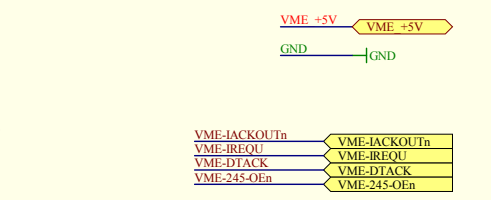
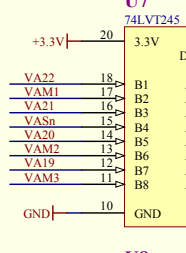
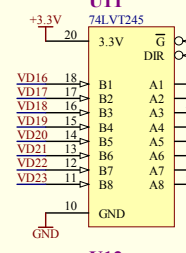
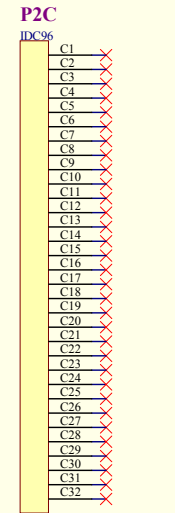
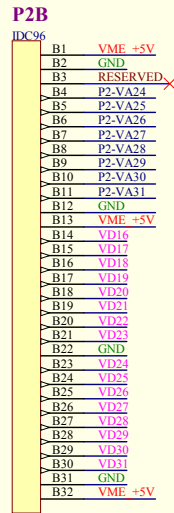
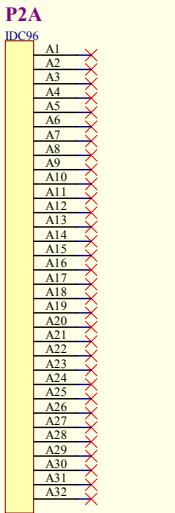
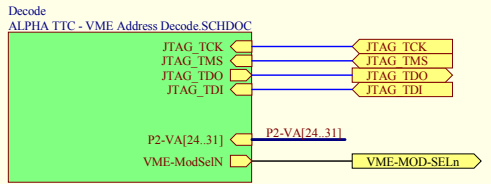
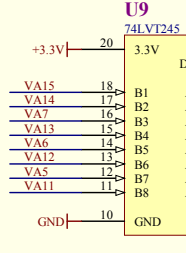
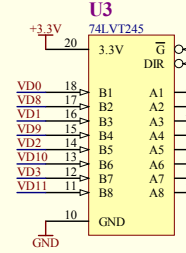
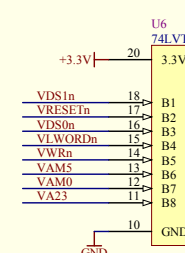
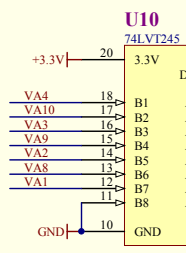
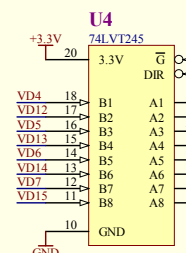
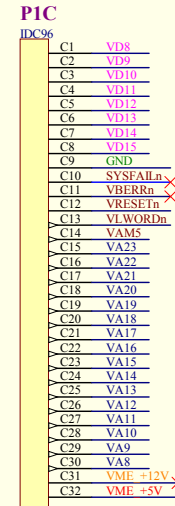
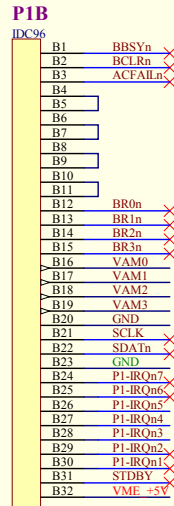
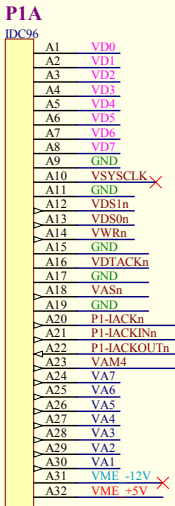
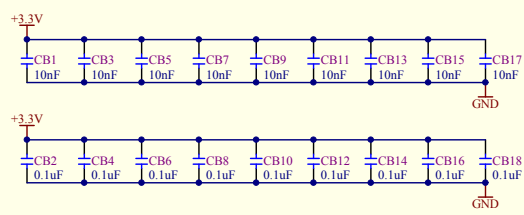
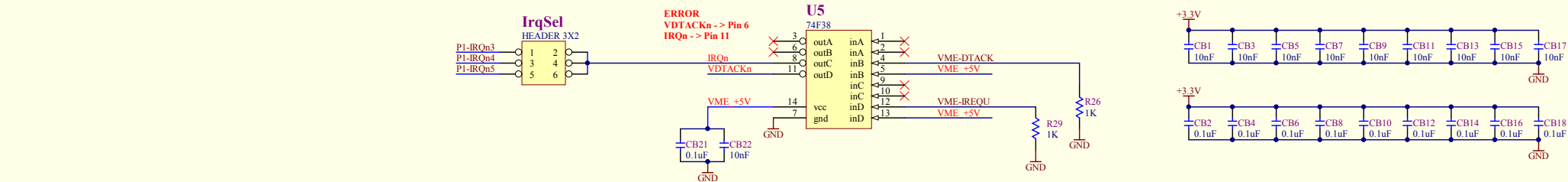
Revision	Drawing #: *	TRUMF
<b>0</b>	Sheet #: 6 of 12 Size: A	4004 Westbrook Mall
	Drawn by: D.Bishop Date: 11/05/2009	Vancouver, B.C.
		Canada
		V6T 2A3
File: G:\AHW\ALPHA\TTC\Altium\ALPHA TTC - LVDS to NIM.SCHDOC		3:34:43 PM

## MICTOR

2-767004-2  
MICTOR 38 pin HP Probe



<b>ALPHA TTC - MICTOR Connector</b>			
<b>0</b>	Revision		Drawing #:
	Sheet #: 7 of 12		Size: A
	Drawn by: D.Bishop		Date: 11/05/2009
File: G:\AHWALPHA\TTC\Altium\ALPHA TTC - MICTOR.SCHDOC			<b>TRIUMF</b> 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3 
			3:34:43 PM



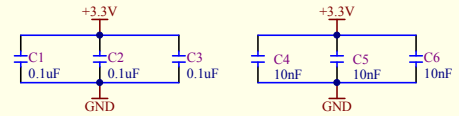
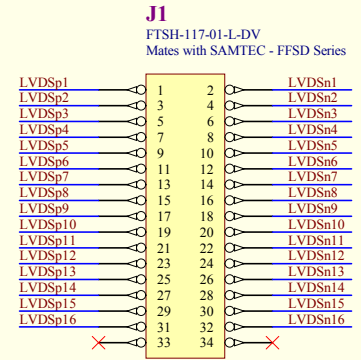
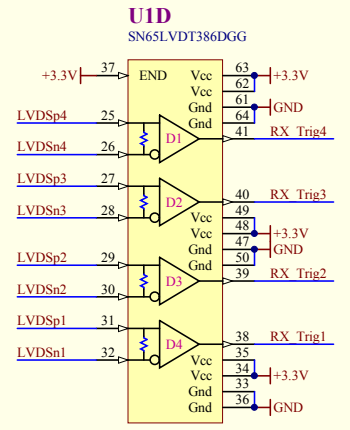
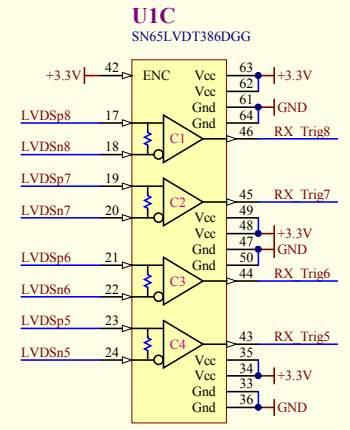
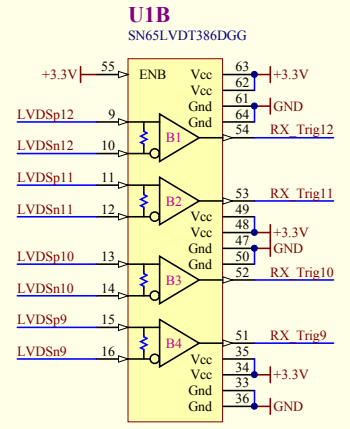
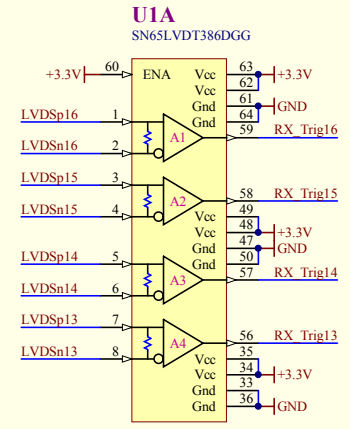
**ALPHA TTC - VME Interface**

Revision	Drawing #:	TRIUMF
0	Sheet # 8 of 12	4004 Wesbrook Mall
Drawn by: Hubert Hui	Date: 11/05/2009	Vancouver, B.C.
File: G:\AH\WALPHA\TTC\Alpha\ALPHA TTC - VME Interface.SchDoc		Canada
		V6T 2A3

3.34:43 PM



RX\_Trig[L.16] → RX\_Trig[L.16]

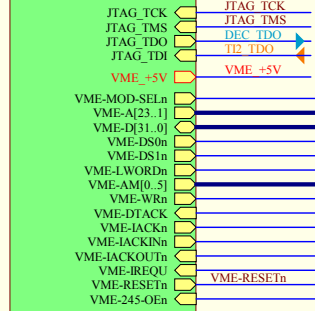


**ALPHA: LVDS Receiver**

Revision	Drawing #:	TRUIMP
0	Sheet # 9 of 12 Size: A	4004 Westbrook Mall
Drawn by: D.Bishop	Date: 11/05/2009	Vancouver, B.C.
		Canada
		V6T 2A3
File: G:\AHW\ALPHA\TTC\Altium\ALPHA TTC - LVDS Receiver.SCHDOC		3:34:43 PM

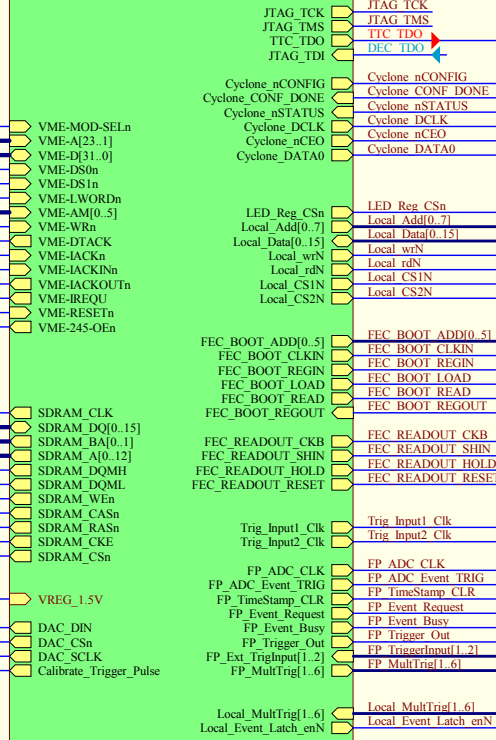
**VME**

ALPHA TTC - VME Interface.SchDoc



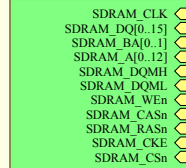
**TTC**

ALPHA TTC - Trigger Logic.SCHDOC



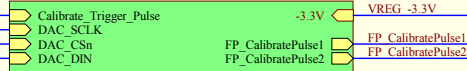
**SDRAM**

ALPHA TTC - SDRAM.SCHDOC



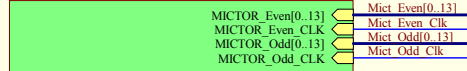
**CAL**

ALPHA TTC - Calibrate Pulse.SCHDOC



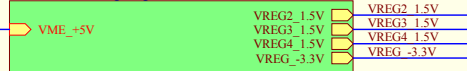
**MICTOR**

ALPHA TTC - MICTOR.SCHDOC



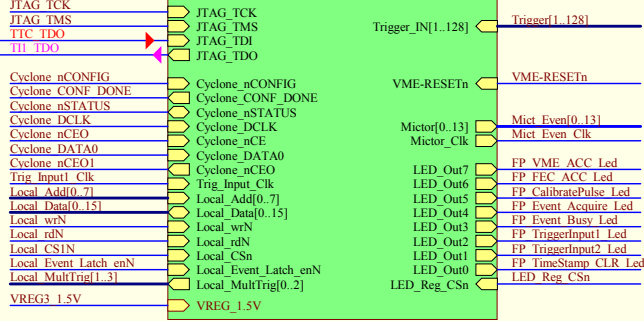
**REG**

ALPHA TTC - Voltage Regulators.SCHDOC



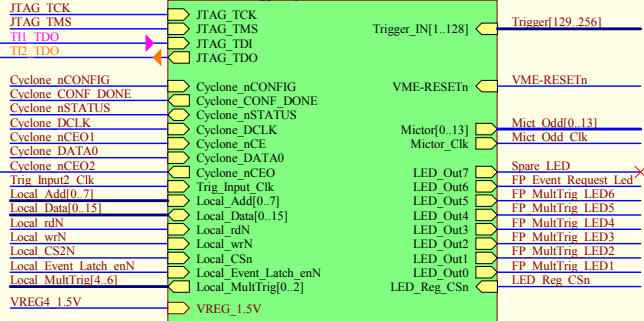
**T11**

ALPHA TTC - Trigger Inputs.SCHDOC



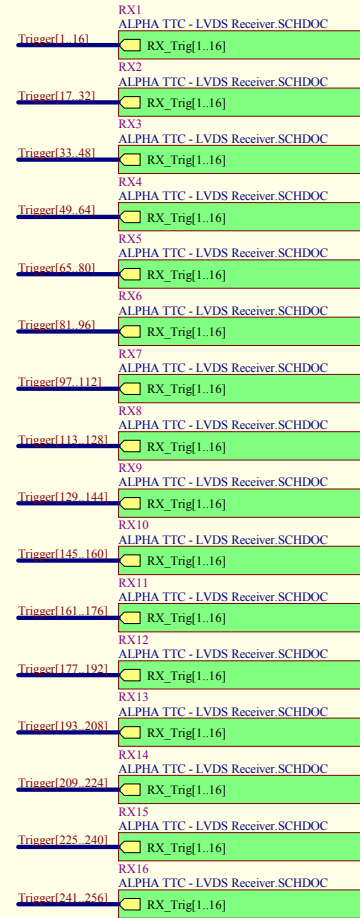
**T12**


ALPHA TTC - Trigger Inputs.SCHDOC

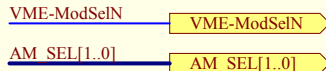


**FP**

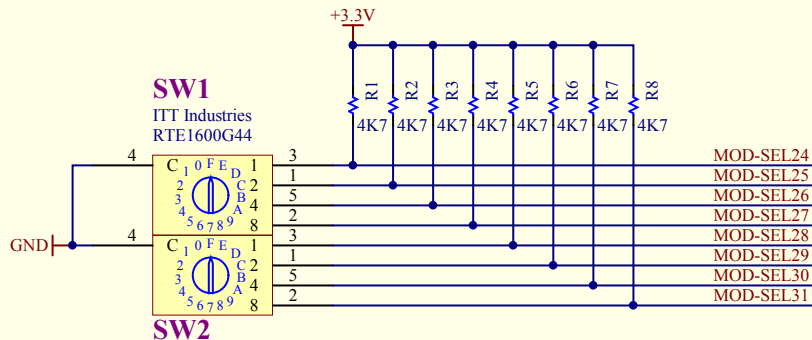
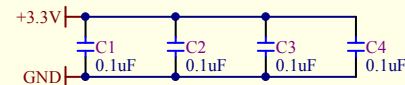
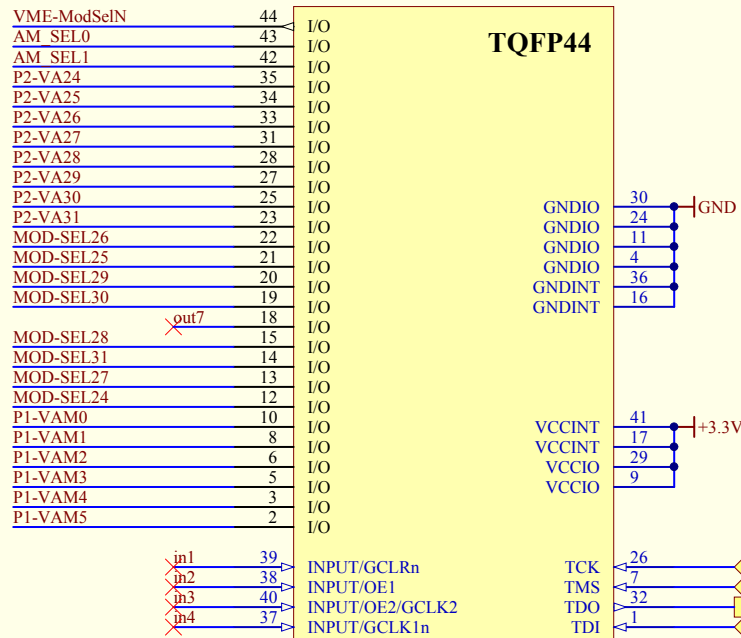
ALPHA TTC - Front Panel.SCHDOC




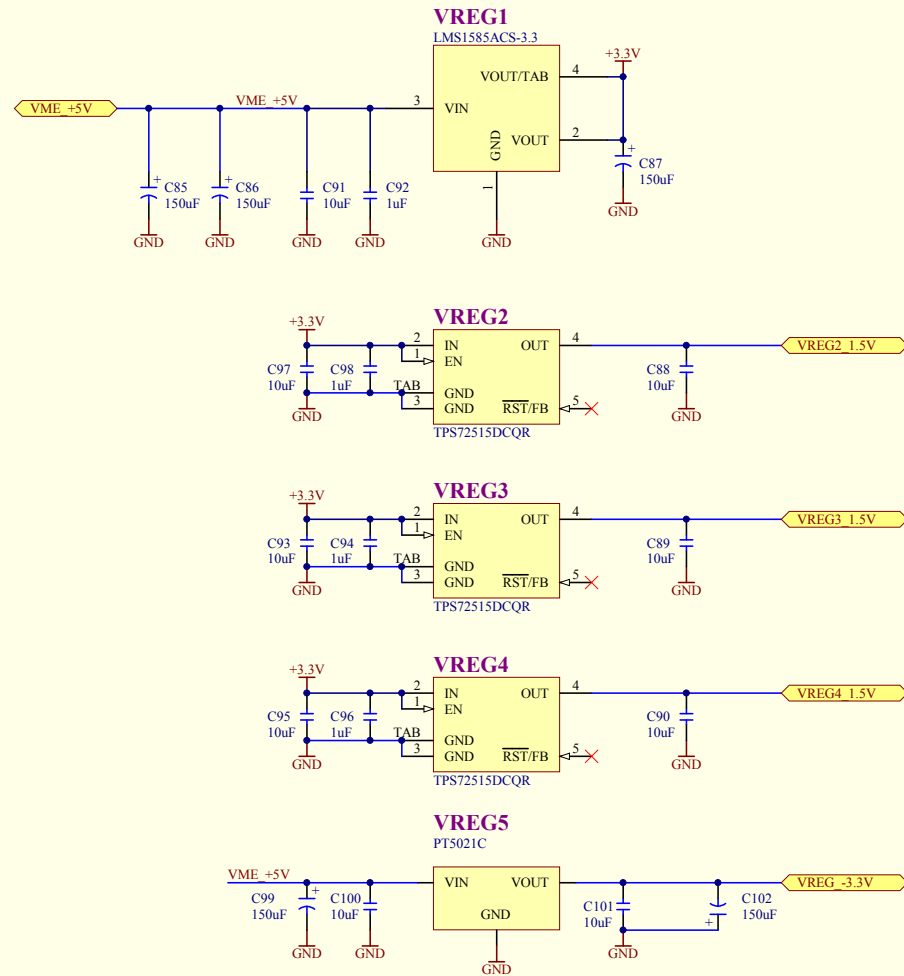
ALPHA TTC - Top Level			
Revision	Drawing #:	TRIUMF 4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3	
0	Sheet #: 10 of 12	Size: B	
Drawn by: D.Bishop	Date: 11/05/2009		
File: G:\AH\WALPHA\TTC\Altim\ALPHA TTC - Top Level.SCHDOC			
3/34/43 PM			




**U1**  
 Altera  
 EPM3032ATC44-7



ALPHA TTC - VME Address Decode			
Revision	Drawing #:		TRIUMF
<b>0</b>	Sheet #: 11 of 12	Size: A	4004 Wesbrook Mall
Drawn by: D.Bishop	Date: 11/05/2009		Vancouver, B.C.
			Canada
			V6T 2A3
File: G:\AHWALPHA\TTC\Altium\ALPHA TTC - VME Address Decode.SCHDOC			
			3:34:43 PM



**ALPHA TTC - Voltage Regulators**

Revision <b>0</b>	Drawing #:	TRIUMF 4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3		
	Sheet #:			Size:
	Drawn by:			Date:
File: G:\AHW\ALPHA\TTC\Altium\ALPHA TTC - Voltage Regulators.SCHDOC		3:34:44 PM		