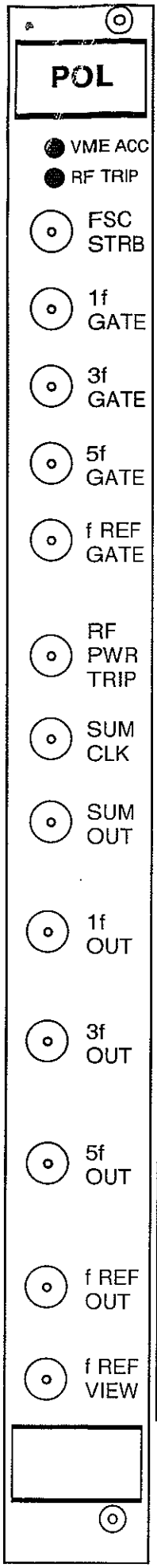

TRIUMF

βNMR VME POL SYNTH Module

General Description

The VME POL SYNTH Module (POL) was designed to generate a complex modulated swept signal summed with a reference frequency. The swept signal may be a single modulated carrier or include the modulated 3rd and 5th harmonics. Each carrier is independently modulated.

The carriers are synthesized and modulated digitally. The modulation data consists of up to 2048 I,Q pairs sampled at a submultiple of the carrier sample rate. The synthesizer circuit interpolates the I,Q sample rate to match the carrier sample rate before modulation.

VME Interface

SLAVE – A24, D16, D8 (OE)

The POL resides in 24-bit address space. Jumpers on the printed circuit board configure the base address selection.

Address Modifier Selection

The POL will only respond to A24 address cycles.
Short supervisory & short nonprivileged access - 0x3D, 0x39

Base Address Selection

Each jumper corresponds to address bits A23 – A16 on the VME address bus. Installing a jumper for each address bit will select a 0 (low) for the corresponding VME address bit.

Table 1 Base Address Selection

Jumpers Installed (X)								Address Range
A23	A22	A21	A20	A19	A18	A17	A16	
X	X	X	X	X	X	X	X	000000 – 00FFFF
-	X	X	X	X	X	X	X	800000 – 80FFFF
-	-	X	X	X	X	X	X	C00000 – C0FFFF
-	-	-	X	X	X	X	X	E00000 – E0FFFF
-	-	-	-	X	X	X	X	F00000 – F0FFFF
-	-	-	-	-	X	X	X	F80000 – F8FFFF
-	-	-	-	-	-	X	X	FC0000 – FCFFFF

Input Signals

Inputs **FSC STRB**, **1f GATE**, **3f GATE**, **5f GATE** and **f REF GATE** are NIM signals. RF Power Trip signal (**RF PWR TRIP**) is an analog signal with maximum input level of 5 volts.

Output Signals

Outputs **1f OUT**, **3f OUT**, **5f OUT**, **f REF OUT** are gated analog signals. **f REF VIEW** is a non-gated **f REF OUT** signal. **SUM OUT** is the analog sum of **1f OUT**, **3f OUT**, **5f OUT** and **f REF OUT** signals. All analog output signals have a maximum output level of ±0.5 volts into 50 ohms. **SUM CLK** is a diagnostic signal and should not be used.

Operating Modes

Single Tone Mode

In this mode the carrier is not modulated. Frequency data is read from the **Frequency Sweep Memory** in the case of the 1f, 3f and 5f channels and from the VME frequency register in the case of the reference channel. Since the 1f, 3f and 5f data is from the **Frequency Sweep Memory** at least one FSC strobe must be issued. If more than one FSC strobe is issued then operation proceeds according to the **Frequency Sweep Memory** description below.

Quadrature Modulation Mode

In Quadrature Mode I and Q data is read from the **I&Q Data Memory**. Each channel has its own memory. If an unmodulated carrier is wanted then the I and Q data are set to constant values. There is a separate length register associated with each **I&Q Data Memory**. When the length is set to zero the last memory location is used as the source of the I and Q data resulting in modulation by a pair of constant values.

Single Frequency

Only the last location (IDLE) in the **Frequency Sweep Memory** is used and at least one FSC strobe must be issued.

Swept Frequency

One 32-bit word is read from the **Frequency Sweep Memory** for each FSC strobe issued starting at the current location.

Functional Blocks

Frequency Sweep Memory

The **Frequency Sweep Memory** has 1024x32-bit frequency values stored in MSB to LSB order as the address increases. The IDLE frequency word must always be initialized. When the sweep reaches the end of the memory as defined by the length register the pointer advances to the IDLE frequency or stops at the Nth frequency according to the setting of the **End Sweep Control** register. For the special case where the length is set to zero the pointer always points to the IDLE frequency.

I&Q Data Memory

The I&Q memory contains the I and Q modulation values stored in alternating locations in MSB to LSB order as the address increases. Each channel has its own memory with 2048x10-bit I&Q data pairs and its own length register. When the GATE signal for a channel goes to the inactive state, its memory pointer is set to the first location. If the GATE remains active for a period longer than the time it takes to read out the memory, as defined by the length register for that channel, then the pointer advances to the IDLE location or stops at the Nth location according to the setting of the **End Sweep Control** register. For the special case where the length is set to zero the pointer always points to the IDLE location and the data pair at that location is used.

In order to increase memory depth, a "buffer factor" ~~N_{IQ}~~ N_C has been implemented. The ~~N_{IQ}~~ N_C value sets the number of I&Q data memory increment pulses to receive from a DDS device before incrementing the I&Q data memory address.

The I and Q data is in 2's complement format.

RF TRIP

The sum output to the RF amplifier is enabled by the **RF PWR TRIP** input. An input from the RF detector exceeding the trip level is latched and disables the **SUM OUT**. The trip latch must be cleared by writing to the **RF Power Status/Trip** register in order to enable the output. A trip will occur if no cable is connected to the input. The trip circuit can be effectively disabled by connecting a 50 ohm terminator in place of the external cable.

GATE Signals

Active levels on the 1f, 3f, 5f, f REF gate signals enable the corresponding RF signals and, in Quadrature Modulation mode, enables the modulation. The modulation data pointer is reset whenever the gate is in the inactive state. Readout begins from the first word each time the gate goes active.

AD9857 Quadrature Upconverter

Sample Rate Interpolation and CIC Filter

The AD9857 combines a Direct Digital Synthesizer (DDS) core with dual multipliers to perform complex modulation using I and Q data loaded into the device. The DDS core generates a new sample at its internal system clock rate, 25ns in this design. The modulated value is computed at the same rate and therefore new I and Q samples must be available at that rate. This rate is much higher than that needed to adequately sample to the modulating waveform and so the AD9857 includes sample rate interpolator which raises the I and Q sample rate to that of the DDS core. This allows the I and Q data to be loaded into the device at a low rate compared to the 25ns system clock.

Before the sample rate can be increased the signal must be band limited or low pass filtered. This is the function of the Comb-Integrator Cascade (CIC) filter. The sample rate can be increased by a factor of 4×(2...63) according to the value in the CIC interpolating rate register. This results in an incoming I&Q data rate of 25ns×4×N where N is between 2 and 63.

Adder and Scaler

The results of the SIN and COS multipliers are summed in the adder and the result multiplied by the 8-bit value loaded in the **Output Scale Factor** register. Due to the effects of scaling within the device a scale factor of B5h gives a full scale output.

Limitations

Maximum frequency sweep strobe rate is 200kHz.

Maximum I&Q data sample rate is 10MHz.

Maximum $N_{I\&Q}$ buffer factor is 32.

The minimum RF trip threshold is approximately 115mV and the maximum is approximately 4.85V.

Reference

AD9857 Quadrature Digital Upconverter Datasheet Rev. B, Analog Devices, 2002.

Table 2 Default Register Values

Function	Address	Value
1f Control Register 1	00	84
1f Control Register 2	01	00
1f Control Register 3	02	08
1f Output Scale Factor	03	B5
1f I&Q Memory Length (MSB)	04	00
1f I&Q Memory Length (LSB)	05	00
1f I&Q Memory Address (MSB)	06	07
1f I&Q Memory Address (LSB)	07	FF
3f Control Register 1	08	84
3f Control Register 2	09	00
3f Control Register 3	0A	08
3f Output Scale Factor	0B	B5
3f I&Q Memory Length (MSB)	0C	00
3f I&Q Memory Length (LSB)	0D	00
3f I&Q Memory Address (MSB)	0E	07
3f I&Q Memory Address (LSB)	0F	FF
5f Control Register 1	10	84
5f Control Register 2	11	00
5f Control Register 3	12	08
5f Output Scale Factor	13	B5
5f I&Q Memory Length (MSB)	14	00
5f I&Q Memory Length (LSB)	15	00
5f I&Q Memory Address (MSB)	16	07
5f I&Q Memory Address (LSB)	17	FF
f Ref Control Register 1	18	84
f Ref Control Register 2	19	00
f Ref Control Register 3	1A	08
f Ref Output Scale Factor	1B	B5
f Ref I&Q Memory Length (MSB)	1C	00
f Ref I&Q Memory Length (LSB)	1D	00
f Ref I&Q Memory Address (MSB)	1E	07
f Ref I&Q Memory Address (LSB)	1F	FF
f Ref Frequency Word 1(MSB)	20	00
f Ref Frequency Word 2	21	00
f Ref Frequency Word 3	22	00
f Ref Frequency Word 4(LSB)	23	00
Frequency Sweep Length (MSB)	24	00
Frequency Sweep Length (LSB)	25	00
Frequency Sweep Address (MSB)	26	03
Frequency Sweep Address (LSB)	27	FF
End Sweep Control	28	1F
RF Trip Threshold	29	80
Frequency Sweep Internal Strobe	2A	00
Frequency Sweep Address Reset	2B	00
Gate Control	2C	55
RF Trip Status/Reset	2D	00
VME Module Reset	2E	00
SPARE	2F	00

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Table 3 Default Register Values

Maximum N_{CMX} Buffer Factor	30	20
N_{C1f} Buffer Factor	31	01
N_{C3f} Buffer Factor	32	01
N_{C5f} Buffer Factor	33	01
N_{Cfref} Buffer Factor	34	01

Table 4 Memory Map

FFFF 9035	UNUSED	
9034 9024	Module Control Registers	10 x 8 bits
9023 9018	f REF Device Registers	12 x 8 bits
9017 9010	5f Device Registers	8 x 8 bits
900F 9008	3f Device Registers	8 x 8 bits
9007 9000	1f Device Registers	8 x 8 bits
8FFF 8000	Frequency Sweep Data Memory	1024 x 32 bits
7FFF 6000	f REF I & Q Data Memory 2's Complement	4096 x 10 bits
5FFF 4000	5f I & Q Data Memory 2's Complement	4096 x 10 bits
3FFF 2000	3f I & Q Data Memory 2's Complement	4096 x 10 bits
1FFF 0000	1f I & Q Data Memory 2's Complement	4096 x 10 bits

Memory areas between 0000h to 8FFFh are uninitialized and not affected by VME resets.

Table 5 Frequency Sweep and I&Q Data Memory Byte Order

Address	I&Q Data	Frequency Data
N+3	Q LSB	Byte 0 (LSB)
N+2	Q MSB	Byte 1
N+1	I LSB	Byte 2
N+0	I MSB	Byte 3 (MSB)

Register Description

All registers respond to byte or word accesses.

1f Control Register 1: 00 (Default: 84h)

ADDR	$xxxx9000 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	1	0	0

bit 7: ***Reserved***

bit 6: ***Reserved***

bit 5: ***PLL Lock Control***

- **0:** device uses PLL Lock Indicator pin to internally control operation of 14-bit parallel data path.
- **1:** internal control logic ignores status at the PLL Lock Indicator pin

bit 4 – 0: ***Reference Clock Multiplier***

- The 5-bit value equals M. If M = 1, the PLL circuit is bypassed and $f_{SYSCLK} = f_{REFCLK}$. If $4 \leq M \leq 20$, then the PLL circuit multiplies f_{REFCLK} by M. All other values of M are invalid.

1f Control Register 2: 01 (Default: 00h)

ADDR	$xxxx9001 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R	R	R/W	R/W	R	R/W
RESET	0	0	0	0	0	0	0	0

bit 7: ***CIC Clear***

- **0:** CIC Filters operate normally.
- **1:** CIC Filters are cleared.

bit 6: ***Inverse SINC Bypass***

- **0:** Inverse SINC Filter is active.
- **1:** Inverse SINC Filter is **BYPASSED**.

bit 5: ***Reserved***

bit 4: ***Reserved***

bit 3: ***Full Sleep Mode***

- **0:** device operates normally.
- **1:** device completely shuts down.

bit 2: ***Auto Power-Down***

- **0:** device only powers down in response to the Digital Power-Down pin.
- **1:** device automatically switches to low-power mode whenever TxENABLE is deasserted for a sufficiently long period.

bit 1: ***Reserved***

bit 0: ***Operating Mode***

- **0:** Quadrature Modulation Mode.
- **1:** Single-Tone Mode

1f Control Register 3: 02 (Default: 08h)

ADDR	$xxxx9002 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	1	0	0	0

bit 7 – 2: ***CIC Interpolating Rate***

00h: Invalid Entry.
01h: CIC Filters **BYPASSED**
02h - 3Fh: CIC interpolation rate (2 - 63, decimal)

bit 1: ***Spectral Invert***

0: quadrature modulation is $I \times \cos(\omega) - Q \times \sin(\omega)$.
1: quadrature modulation is $I \times \cos(\omega) + Q \times \sin(\omega)$.

bit 0: ***Inverse CIC Bypass***

0: Inverse CIC Filter is active.
1: Inverse CIC Filter is **BYPASSED**.

1f Output Scale Factor Register: 03 (Default: B5h)

ADDR	$xxxx9003 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	1	0	1	0	1

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

1f I&Q Data Memory Length Register: 04, 05 (Default: 0000h)

ADDR	$xxxx9004 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx9005 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

1f I&Q Data Memory Address Register: 06, 07 (Default: 07FFh)

ADDR	$xxxx9006 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	1	1	1

ADDR	$xxxx9007 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	1	1	1	1	1	1	1

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

3f Control Register 1: 08 (Default: 84h)

ADDR	$xxxx9008 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	1	0	0

bit 7: ***Reserved***

bit 6: ***Reserved***

bit 5: ***PLL Lock Control***

- **0:** device uses PLL Lock Indicator pin to internally control operation of 14-bit parallel data path.
- **1:** internal control logic ignores status at the PLL Lock Indicator pin

bit 4 – 0: ***Reference Clock Multiplier***

- The 5-bit value equals M. If M = 1, the PLL circuit is bypassed and $f_{SYSCLK} = f_{REFCLK}$. If $4 \leq M \leq 20$, then the PLL circuit multiplies f_{REFCLK} by M. All other values of M are invalid.

3f Control Register 2: 09 (Default: 00h)

ADDR	$xxxx9009 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R	R	R/W	R/W	R	R/W
RESET	0	0	0	0	0	0	0	0

bit 7: ***CIC Clear***

- **0:** CIC Filters operate normally.
- **1:** CIC Filters are cleared.

bit 6: ***Inverse SINC Bypass***

- **0:** Inverse SINC Filter is active.
- **1:** Inverse SINC Filter is **BYPASSED**.

bit 5: ***Reserved***

bit 4: ***Reserved***

bit 3: ***Full Sleep Mode***

- **0:** device operates normally.
- **1:** device completely shuts down.

bit 2: ***Auto Power-Down***

- **0:** device only powers down in response to the Digital Power-Down pin.
- **1:** device automatically switches to low-power mode whenever TxENABLE is deasserted for a sufficiently long period.

bit 1: ***Reserved***

bit 0: ***Operating Mode***

- **0:** Quadrature Modulation Mode.
- **1:** Single-Tone Mode

3f Control Register 3: 0A (Default: 08h)

ADDR	$xxxx900A (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	1	0	0	0

bit 7 – 2: ***CIC Interpolating Rate***

00h: Invalid Entry.
01h: CIC Filters **BYPASSED**
02h - 3Fh: CIC interpolation rate (2 - 63, decimal)

bit 1: ***Spectral Invert***

0: quadrature modulation is $I \times \cos(\omega) - Q \times \sin(\omega)$.
1: quadrature modulation is $I \times \cos(\omega) + Q \times \sin(\omega)$.

bit 0: ***Inverse CIC Bypass***

0: Inverse CIC Filter is active.
1: Inverse CIC Filter is **BYPASSED**.

3f Output Scale Factor Register: 0B (Default: B5h)

ADDR	$xxxx900B (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	1	0	1	0	1

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

3f I&Q Data Memory Length Register: 0C, 0D (Default: 0000h)

ADDR	$xxxx900C (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx900D (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

3f I&Q Data Memory Address Register: 0E, 0F (Default: 07FFh)

ADDR	$xxxx900E (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	1	1	1

ADDR	$xxxx900F (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	1	1	1	1	1	1	1

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

5f Control Register 1: 10 (Default: 84h)

ADDR	$xxxx9010 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	1	0	0

bit 7: ***Reserved***

bit 6: ***Reserved***

bit 5: ***PLL Lock Control***

- **0:** device uses PLL Lock Indicator pin to internally control operation of 14-bit parallel data path.
- **1:** internal control logic ignores status at the PLL Lock Indicator pin

bit 4 – 0: ***Reference Clock Multiplier***

- The 5-bit value equals M. If M = 1, the PLL circuit is bypassed and $f_{SYSCLK} = f_{REFCLK}$. If $4 \leq M \leq 20$, then the PLL circuit multiplies f_{REFCLK} by M. All other values of M are invalid.

5f Control Register 2: 11 (Default: 00h)

ADDR	$xxxx9011 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R	R	R/W	R/W	R	R/W
RESET	0	0	0	0	0	0	0	0

bit 7: ***CIC Clear***

- **0:** CIC Filters operate normally.
- **1:** CIC Filters are cleared.

bit 6: ***Inverse SINC Bypass***

- **0:** Inverse SINC Filter is active.
- **1:** Inverse SINC Filter is **BYPASSED**.

bit 5: ***Reserved***

bit 4: ***Reserved***

bit 3: ***Full Sleep Mode***

- **0:** device operates normally.
- **1:** device completely shuts down.

bit 2: ***Auto Power-Down***

- **0:** device only powers down in response to the Digital Power-Down pin.
- **1:** device automatically switches to low-power mode whenever TxENABLE is deasserted for a sufficiently long period.

bit 1: ***Reserved***

bit 0: ***Operating Mode***

- **0:** Quadrature Modulation Mode.
- **1:** Single-Tone Mode

5f Control Register 3: 12 (Default: 08h)

ADDR	$xxxx9012 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	1	0	0	0

bit 7 – 2: ***CIC Interpolating Rate***

00h: Invalid Entry.
01h: CIC Filters **BYPASSED**
02h - 3Fh: CIC interpolation rate (2 - 63, decimal)

bit 1: ***Spectral Invert***

0: quadrature modulation is $I \times \cos(\omega) - Q \times \sin(\omega)$.
1: quadrature modulation is $I \times \cos(\omega) + Q \times \sin(\omega)$.

bit 0: ***Inverse CIC Bypass***

0: Inverse CIC Filter is active.
1: Inverse CIC Filter is **BYPASSED**.

5f Output Scale Factor Register: 13 (Default: B5h)

ADDR	$xxxx9013 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	1	0	1	0	1

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

5f I&Q Data Memory Length Register: 14, 15 (Default: 0000h)

ADDR	$xxxx9014 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx9015 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

5f I&Q Data Memory Address Register: 16, 17 (Default: 07FFh)

ADDR	$xxxx9016 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	1	1	1

ADDR	$xxxx9017 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	1	1	1	1	1	1	1

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

f REF Control Register 1: 18 (Default: 84h)

ADDR	$xxxx9018 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	1	0	0

bit 7: ***Reserved***

bit 6: ***Reserved***

bit 5: ***PLL Lock Control***

- **0:** device uses PLL Lock Indicator pin to internally control operation of 14-bit parallel data path.
- **1:** internal control logic ignores status at the PLL Lock Indicator pin

bit 4 – 0: ***Reference Clock Multiplier***

- The 5-bit value equals M. If M = 1, the PLL circuit is bypassed and $f_{SYSCLK} = f_{REFCLK}$. If $4 \leq M \leq 20$, then the PLL circuit multiplies f_{REFCLK} by M. All other values of M are invalid.

f REF Control Register 2: 19 (Default: 00h)

ADDR	$xxxx9019 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R	R	R/W	R/W	R	R/W
RESET	0	0	0	0	0	0	0	0

bit 7: ***CIC Clear***

0: CIC Filters operate normally.
1: CIC Filters are cleared.

bit 6: ***Inverse SINC Bypass***

0: Inverse SINC Filter is active.
1: Inverse SINC Filter is **BYPASSED**.

bit 5: ***Reserved***

bit 4: ***Reserved***

bit 3: ***Full Sleep Mode***

0: device operates normally.
1: device completely shuts down.

bit 2: ***Auto Power-Down***

0: device only powers down in response to the Digital Power-Down pin.
1: device automatically switches to low-power mode whenever TxENABLE is deasserted for a sufficiently long period.

bit 1: ***Reserved***

bit 0: ***Operating Mode***

0: Quadrature Modulation Mode.
1: Single-Tone Mode

f REF Control Register 3: 1A (Default: 08h)

ADDR	$xxxx901A (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	1	0	0	0

bit 7 – 2: ***CIC Interpolating Rate***

00h: Invalid Entry.
01h: CIC Filters **BYPASSED**
02h - 3Fh: CIC interpolation rate (2 - 63, decimal)

bit 1: ***Spectral Invert***

0: quadrature modulation is $I \times \cos(\omega) - Q \times \sin(\omega)$.
1: quadrature modulation is $I \times \cos(\omega) + Q \times \sin(\omega)$.

bit 0: ***Inverse CIC Bypass***

0: Inverse CIC Filter is active.
1: Inverse CIC Filter is **BYPASSED**.

f REF Output Scale Factor Register: 1B (Default: B5h)

ADDR	$xxxx901B (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	1	0	1	0	1

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

f REF I&Q Data Memory Length Register: 1C, 1D (Default: 0000h)

ADDR	$xxxx901C (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx901D (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

f REF I&Q Data Memory Address Register: 1E, 1F (Default: 07FFh)

ADDR	$xxxx901E (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	1	1	1

ADDR	$xxxx901F (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	1	1	1	1	1	1	1

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

f REF Frequency Tuning Registers: 20, 21, 22, 23 (Default: 00000000h)

ADDR	$xxxx9020 (Bits 31-24)							
BIT	31	30	29	28	27	26	25	24
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx9021 (Bits 23-16)							
BIT	23	22	21	20	19	18	17	16
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx9022 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx9023 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

f_{OUT} = (Frequency Tuning Word × 40×10^6) / 2^{32}

Frequency is updated once register 23h is written.

Frequency Sweep Memory Length Register: 24, 25 (Default: 0000h)

ADDR	$xxxx9024 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADDR	$xxxx9025 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The 10-bit value is the number of valid 32-bit frequency tuning values stored in the Frequency Sweep memory.

Frequency Sweep Memory Address Register: 26, 27 (Default: 03FFh)

ADDR	$xxxx9026 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	1	1

ADDR	$xxxx9027 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	1	1	1	1	1	1	1

The 10-bit value is the current address pointer into the Frequency Sweep memory. The default value points to the IDLE frequency.

End Sweep Control Register: 28 (Default: 1Fh)

ADDR	$xxxx9028 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	1	1	1	1	1

bits 7 - 5: ***Reserved***

bit 4: ***Frequency Sweep End Sweep Mode***
0: stop at Nth if strobes or gate exceed length
1: jump to IDLE if strobes or gate exceed length.

bit 3: ***f REF I&Q End Sweep Mode***
0: stop at Nth if strobes or gate exceed length
1: jump to IDLE if strobes or gate exceed length.

bit 2: ***5f I&Q End Sweep Mode***
0: stop at Nth if strobes or gate exceed length
1: jump to IDLE if strobes or gate exceed length.

bit 1: ***3f I&Q End Sweep Mode***
0: stop at Nth if strobes or gate exceed length
1: jump to IDLE if strobes or gate exceed length.

bit 0: ***1f I&Q End Sweep Mode***
0: stop at Nth if strobes or gate exceed length
1: jump to IDLE if strobes or gate exceed length.

RF Power Trip Threshold Register: 29 (Default: 80h)

ADDR	$xxxx9029 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	0	0	0

8-bit value determines the RF Power trip level.

V_{TRIP} = 5 volts × 8-bit value / 255

Frequency Sweep Internal Strobe Register: 2A (Default: 00h)

ADDR	$xxxx902A (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Write cycle will load into the **1f**, **3f** and **5f** DDS device the frequency pointed to by the **Frequency Sweep Memory Address** register.

Frequency Sweep Memory Address Reset Register: 2B (Default: 00h)

ADDR	$xxxx902B (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Write cycle will reset DDS Frequency Sweep Memory Address pointer registers (26h,27h) to the default value and loads the IDLE frequency into the DDS device.

Gate Control Register: 2C (Default: 55h)

ADDR	$xxxx902C (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	1	0	1	0	1	0	1

bit 1 - 0: ***1f Gate Control***
bit 3 - 2: ***3f Gate Control***
bit 5 - 4: ***5f Gate Control***
bit 7 - 6: ***f Ref Gate Control***

00b: front panel gate input disabled
01b: normal mode (Default)
10b: gate pulse inverted
11b: front panel gate input ignored and internal gate always ON

RF Power Status/Trip Reset Register: 2D (Default: 00h)

ADDR	$xxxx902D (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

bit 0: ***RF Power Trip Indicator***
0: normal operation
1: **SUM OUT** tripped

Write cycle will clear RF Power Trip latch.

VME Module Reset Register: 2E (Default: 00h)

ADDR	$xxxx902E (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Write cycle will reset all VME registers and all DDS device registers to default values. Memory locations will be unaffected.

N_{CMX} Buffer Factor Register: 30 (Default: 20h)

ADDR	$xxxx9030 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	1	0	0	0	0	0

This register sets the upper limit of the I&Q data memory increment pulses to receive from a DDS device before incrementing the I&Q data memory address.

N_{C1f} Buffer Factor Register: 31 (Default: 01h)

ADDR	$xxxx9031 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	1

In Quadrature Mode, this 6-bit value sets the number of I&Q data memory increment pulses to receive from the 1f DDS device before incrementing the I&Q data memory address.

Valid range: $1 \leq N_{C1f} \leq$ Maximum N_{CMX} (register 30)

N_{C3f} Buffer Factor Register: 32 (Default: 01h)

ADDR	$xxxx9032 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	1

In Quadrature Mode, this 6-bit value sets the number of I&Q data memory increment pulses to receive from the 3f DDS device before incrementing the I&Q data memory address.

Valid range: $1 \leq N_{C3f} \leq$ Maximum N_{CMX} (register 30)

N_{C5f} Buffer Factor Register: 33 (Default: 01h)

ADDR	$xxxx9033 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	1

In Quadrature Mode, this 6-bit value sets the number of I&Q data memory increment pulses to receive from the 5f DDS device before incrementing the I&Q data memory address.

Valid range: $1 \leq N_{C5f} \leq$ Maximum N_{CMX} (register 30)

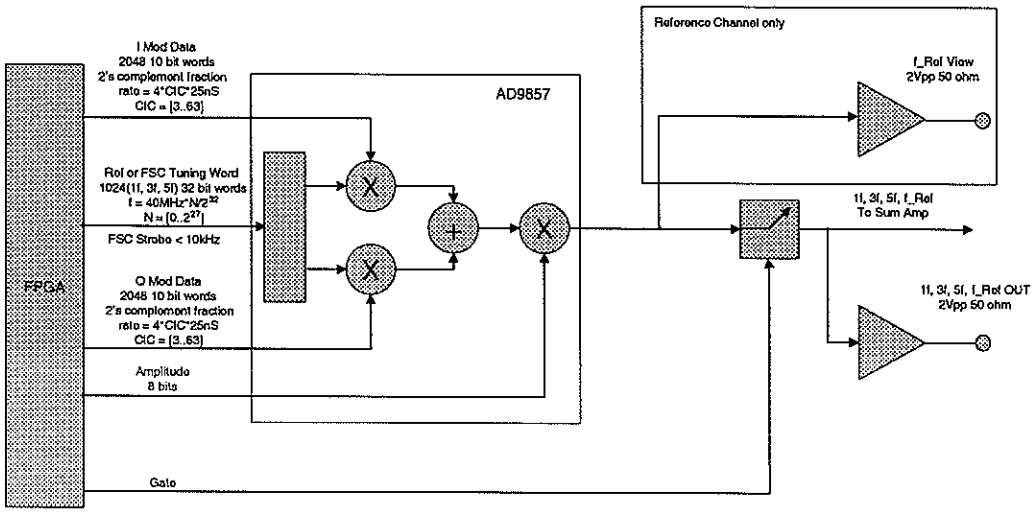
N_{Cfref} Buffer Factor Register: 34 (Default: 01h)

ADDR	$xxxx9034 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	1

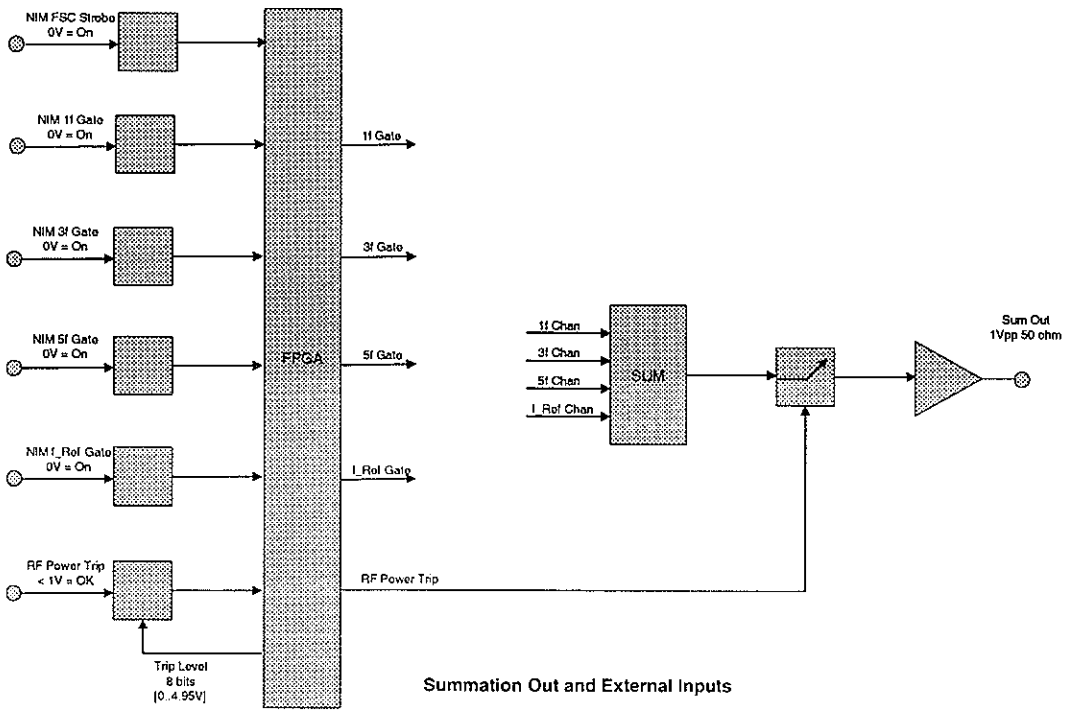
In Quadrature Mode, this 6-bit value sets the number of I&Q data memory increment pulses to receive from the f Ref DDS device before incrementing the I&Q data memory address.

Valid range: $1 \leq N_{Cfref} \leq$ Maximum N_{CMX} (register 30)

Block Diagram of Module Operation



1f, 3f, 5f, Reference Channels



Summation Out and External Inputs

Revision History

Rev Nov 20/2003	...	original spec
Rev Dec 1 /2003	...	added functions idle_freq idle_iq added detailed procedure to calculate the frequency sweep values
Rev Feb 26/2004	...	added gate control logic into register 2C and moved old 2C functions to 2D, old 2D function to 2E (see * lines)
Rev May 10/2004	...	added section on how to do the complex modulation; srk
Rev July 19/2004	...	corrected and updated complex modulation section; srk
Rev Sept 10/2004	...	added functionality for iq data recycling by introducing five new Registers Ncmx, Nc1f, Nc3f, Nc5f, Ncfref into locations 30-31 Also introduced the modulation function parameters A and a to define the modulation function properties (i.e. linewidth and ending ampliture).

Local Control Register Level Functionality

Function	Value	Register	Access
1f-qm-on	0x	01	r/w
1f-qm-off	1x	01	r/w
1f-cic	2-ffx	02	r/w
1f-scale	0x-ffx	03	r/w
1f-n_iq	0x-7ffx	04-05	r/w
1f-iq_ptr		06-07	r only
1f-on	1,1b	2C bits 0,1	r/w
1f-off	0,0b	2C bits 0,1	r/w
1f-gate-t	1,0b	2C bits 0,1	r/w
1f-gate-f	0,1b	2C bits 0,1	r/w
Nc1f	1x-01x	31 bits 0-5	r/w 0x is not allowed
3f-qm-on	0x	09	r/w
3f-qm-off	1x	09	r/w
3f-cic	2-ffx	0A	r/w
3f-scale	0x-ffx	0B	r/w
3f-n_iq	0x-7ffx	0C-0D	r/w
3f-iq_ptr		0E-0F	r only
3f-on	1,1b	2C bits 2,3	r/w
3f-off	0,0b	2C bits 2,3	r/w
3f-gate-t	1,0b	2C bits 2,3	r/w
3f-gate-f	0,1b	2C bits 2,3	r/w
Nc3f	1x-01x	32 bits 0-5	r/w 0x is not allowed
5f-qm-on	0x	11	r/w
5f-qm-off	1x	11	r/w
5f-cic	2-ffx	12	r/w
5f-scale	0x-ffx	13	r/w
5f-n_iq	0x-7ffx	14-15	r/w
5f-iq_ptr		16-17	r only
5f-on	1,1b	2C bits 4,5	r/w
5f-off	0,0b	2C bits 4,5	r/w
5f-gate-t	1,0b	2C bits 4,5	r/w
5f-gate-f	0,1b	2C bits 4,5	r/w
Nc5f	1x-01x	33 bits 0-5	r/w 0x is not allowed
fref-qm-on	0x	19	r/w

fref-qm-off	1x	19	r/w
fref-cic	2-ffx	1A	r/w
fref-scale	0x-ffx	1B	r/w
fref-n_iq	0x-7ffx	1C-1D	r/w
fref-iq_ptr		1E-1F	r only
fref-on	1,1b	2C bits 6,7	r/w
fref-off	0,0b	2C bits 6,7	r/w
fref-gate-t	1,0b	2C bits 6,7	r/w
fref-gate-f	0,1b	2C bits 6,7	r/w
Ncfref	1x-01x	34 bits 0-5	r/w 0x is not allowed
fref-freqx	0-ffffffffx	20-23	r/w write order: 20 first 23 last

fref-freqx = (fref_Hz*2^32/(4x10^7))x=(fref_Hz*(107.3741824))x=(fref_Hz/finc)x
finc = .009313226Hz
fmax = 4*10^7 - finc

n_fsweep	0-3ff	24-25	r/w
fsweep_ptr		26-27	r only
iq-end_idle	?fx	28 bits 1-4only	r/w
iq-end_niq	?0x	28 bits 1-4 only	r/w
fsweep-end_idle	1?x	28 bit 5 only	r/w
fsweep-end_nfsweep	0?x	28 bit 5 only	r/w

or reg_28x = (iq-end*0fx)+(sweep-end*10x),
where iq-end is 1 (iq-end_idle) or 0 (iq-end_niq)
and sweep-end is 1 (sweep-end_idle) or 0 (sweep-end_nfsweep).
reg_28x is calculated and written whenever the values of iq-end or sweep-end are changed.

RF_power_trip_thr	0-ffx	29	r/w
fsweep_int_strobe	0		w, r is always 0
fsweep_ptr_reset	0	2b	w, r is always 0
RF_power_trip_stat	0	2d	w cycle will reset, read is 1 or 0
VME_reset	0	2e	w cycle resets all vms and DDS registers to default
Ncmx	1x	30 max number of cycles available to cycle the iq pairs	

Global Control Functions

qm-on > 1f-qm-on,3f-qm-on,5f-qm-on,frfef-qm-on
qm-off > 1f-qm-off,3f-qm-off,5f-qm-off,frfef-qm-off
n_iq 0x-7ffx > 1f-n_iq,3f-n_iq,5f-n_iq,frfef-n_iq all set to same value, default value is 2048 = 8FFx
iq_ptr displays all 1r,3f,5f,fref-iq_ptr
cic_ir 2-ffx > 1f-cic, 3f-cic, 5f-cic, fref-cic all set to same value
idle_freq (specify and load the value of idle_freq into 8FFC-F)
idle_iq (specify and load the i and q modulation default values into 1/3/5/7FFC-F)
Nc 1x-01x > Nc1f, Nc3f, Nc5f, Ncfref all set to same value Nc

Freq Sweep Loading

fsweep 0-ffffffffx	8000-8FFC	r/w n_fsweep locations to to loaded
	8FFD-8FFF	r/w + the idle frequence

It is probably best to divide the freq steps into multiples of finc, so determine the closest start freq, the closest value of the requested freq step in units of finc (call this delta_fincx) and the number of dealta_fincs required to get to withing 1/2 finc of the requested ending frequency. Then you can program the first location with the closest intitial start frequency, and a delta_fincx to that value successively for each 32bit frequency word. This means that the actual start, stop, and step frequencies are computed as well as the number (i.e. n_fsweep) steps to get there. These number will be slightly different than what the user requested ... but the frequency increments will be absolutely constant. The calculation of the frequency is the same as that indicated for fref_freq. See detailed instructions below.

IQ data	0000-1FFF	}
	2000-3FFF	} All sets of registers are loaded with same set of data.
	4000-5FFF	} The 1/3/5/7FFE - 1/3/5/7FFF locations are always loaded
	6000-7FFF	} with the idle I/Q data pair.

Detailed notes to for frequency sweep programming:

i) Determine the actual_start_frequency, it will be the closest frequency to the requested start_freq

ii) Determine the actual_frequency_step, it will the frequency closest to the requested freq_step

iii) Determfine the actual_number_freq_steps to get to the first frequency beyond the requested stop_freq

iv) Compute the actual_stop_frequency

actual_start_frequencyx = (int(start_frequency/finc))x
actual_start_frequency_hz =(int(start_frequency/finc))*finc

actual_frequency_stepx = (int(freq_step)/finc))x
actual_frequency_step_hz = (int(frq_step)/finc))*finc

actual_number_freq_steps = int((stop _freq - start_freq)/actual_frequency_step_hz)
actual_stop_freq_hz = actual_start_freq_hz + actual_number_freq_steps*actual_freq_step

a) into location 8000 put the actual_start_frequencyx according to table 4 on page 6 of the manual (t4p6)

b) into location 8000x+(4*n)x put actual_start_frequencyx +nx*actual_frequency_stepx according to t4p6, for all n's 1 to actual_number_freq_steps

c) may be accoplished in two ways. You can use the fact that the n=1'th frequency data in location 8000x+(4*(n+1))x is the data in location 8000x+(4*n)x + actual_frequency_stepx

I suggest that a table of the all the actual_frequency_n be calculated, both in hz and in binary (i.e. hex) which then can be read into the memory according to order specified in t4p6. This give one a chance to look at the table for debugging purposes. Donald thinks that data should just be programmed in on the fly.

IQ modulation programing:

Perscription for complex Ln-Sech modulation:

(this can be used as a template for other modulation functions, the explanation of why the prescription is what it is follows at the end ... it should then be clearer on how to make the presciption for other modulation functions)

0) Select the modulation function and input the parameters A & alpha
ln-sech is used below and it's A/a parameters are .1 and 5 respectively.

1) Input the requested dnu (in Hz) and define dw=dnu*2*pi
(d_nu is the requested bandwidth (in Hz) that the modulation function will irradiate given a proper level of RF power) 5 0.1

2) Define dw_max=10^(9) a / (10 A * 512 * 2)=4882.5*10^3 radians/sec
dw_min= dw_max / (128 Ncmx) = 38.75*10^3/Ncmx
d_nu_min = dw_min/(2*pi) , d_nu_max = dw_max/(2*pi)

3) Check that d_nu_min <= d_nu <= d_nu_max, else return an error stating that the requested d_nu in not with the available limits ... say what these limits are.

4) Compute the preliminary total number of iq points Ntiqtemp
Ntiqtemp = dw*A*Ntqitemp*20*2={ a * 2 *10^(9) / (20 *A *dw) } = {(5*10^9)/dw},
{ ... } = nearest smaller integer,
and confirm that 1024<= Ntiqtemp < 129024*Ncmx.

$$\frac{1}{\frac{5\times 2\times 10^{9}}{2426\times 0.1\times dw}} = \frac{5\times 10^{9}}{dw}$$

5) Assign Nc and Ncic according to the following table:

Ntiqtemp	Nc	Ncic
1024 - 2047	1	2
2048 - 4095	1	2
4096 - 8191	1	4
8192 - 16383	1	8
16384 - 32767	1	16
32768 - 65535	1	32
65536 - 129023	1	63
129024 - 258047	2	63
258048 - 516095	4	63
516096 - 1032191	8	63
1032192 - 2064383	16	63
2064384 - 4128767	32	63

Confirm that Nc <= Ncmx.

6) Compute Niq and Ntiq
Niq=[Ntiqtemp/(Nc*Ncic)] , [...] = nearest larger integer ; Ntiq = Niq*Nc*Ncic
For consistency check, 512<= Niq <= 2048, and Ntiq < 129024*Ncmx;
if they are not then the explanation/calculation below/above is inconsistent and needs to be corrected/debugged.

7) Program Niq as the argument of the n_iq function.
Program Nc and Ncic as the arguments of the Nc and icc_ir functions respectively.

8) Calculate tp :
   tp = 20*10^(-9)*Ntiq
   This value of the pulse width must be programmed into the PPG as the RFon time.

9) Compute for n=1 to Niq :
   a(n)=sech({dw*Tp/10}*{n/Niq - 1/2})
   phi(n)=5*ln(a(n))
   I(n)= <511*a(n)*cos(phi(n))> , <...> means closest integer
   Q(n)= <511*a(n)*sin(phi(n))>

10) Store the I(n),Q(n) data set in decimal and 2's compliment

11) Use the 2's compliment data pairs of (I(n),Q(n)) for n=1 -> Niq
    for the n_iq function (which loads identical iq data for all the frequencies).

Explanation of iq modulation prescription:

(Indented text describes the specific case for ln-sech case.)

i) Chose a functional shape. It can always be expressed as f(dw*A*(t-tp/2)), for 0<=t<=tp, defining the pulse width tp, the band width dw and a scaling factor A. It is assumed that f(0)=1, f(t>0)<1, and f(dw*A*tp/2)<<1 . The reason for the last constraint is so that the RF power turns off properly within the defined pulse shape, otherwise power harmonics at other (non-desirable) frequencies will be introduced into the system at the end of the rf-gate.

For the ln-sech mod function the complex modulation function is
w1(t) = w1_max* (sech(b*t)^(1+i*u) , i^2=-1
or
w1(t) = w1_max*(sech(b*t))*exp^(i*phi(b*t)) & phi(b*t) = u*ln(sech(b*t))
The irradiated line width is dw=2*u*b (i.e. between +- u*b) and a value of u=5 is a good value which delivers a fairly nice selective rectangular frequency selection slice. Therefore the pulse shape is
f=sech(dw*.1*(t-tp/2))^(1+iu), for 0<=t<=tp . i.e. A=.1 $\leftarrow \frac{1}{2\pi} \approx .1$

Let Niq be the number of digitized iq pairs. The maximum Niq is 2048, and we impose a minimum Niq of 512 to get decent modulation shape resolution/faithfulness. Each Niq pair is read (and interpolated) into the dsp in Ncic*Nc nanoseconds. Thus the entire modulation pulse width is tp=10^(-9)*Niq*Ncic*Nc. Where Nc is the number of times (cycles) each iq pair is repeated as it is fed from the iq memory into the dsp modulation digitizers. The total number of 20ns points is Ntiq= Niq*Ncic*Nc and the form of the function in iq memory is iq(n) = <511*f(dw*A*(n - Niq/2))>, The constant 511 reflects a 10 bit bipolar amplitude programmable in binary 2's compliment format.

For the ln-sech function the data in iq memory looks like
iq(n) = <511{sech((dw*tp/10)*(n/Niq - .5))}^{1+i5}>,
= <511{sech((dw*Ncic*Nc*Niq*20*10^(-9)/10)*(n/Niq - .5))}^{1+i5}>

To chose Ncic, Nc, and Niq first requires relating the band width/shape of the modulation function to the pulse length. Then an approximate Ntiqtemp is determined so that at n=Niq (t=tp) the function is small. From the value of Ntiqtemp, Ncic and Nc can be determined from a table (in the previous section) and then the value of Niq (and therefore Ntiq and tp) can be determined.

ii) Ntiqtempt calculation: Define a so that the value of f(a)<=.015
Then Ntiqtemp is defined so that dw*A*Ntqitemp*20*10^(-9)/2=a. i.e.
Ntiqtemp = dw*A*Ntqitemp*20*2={ a * 2 *10^(9) / (20 *A *dw) } = {(5*10^9)/dw},
{ ... } = nearest smaller integer,
(For the ln-sech function we use a=5, i.e. sech(5) ~.013, which is fine.)

$$\left[A\, dw\, N_{cic}\, N_c\, N_{iq}\, 10^{-7}\right]\left[(n/N_{iq} - .5)^{.5}\right] = \alpha$$

$$N_{tiqt} = \frac{10^7 2\alpha}{A\, dw}$$

iii) Pick Ncic and Nc from the table. This table was produced to chose the best combination of Ncic*Nc*Niq that will deliver a faithful modulation pulse. As a guideline we tried to keep Niq reasonably high to yield good resolution in the modulation line shape. However, if dw is sufficiently high, then one requires smaller Ncic*Nc*Niq to do the job. Using the guideline that the minimum acceptable Niq is 512 then the product of Niq*Nc*Niq can be categorized as in the table to cover the entire dynamic range

Ntiqtemp	Nc	Ncic
1024 - 2047	1	2
2048 - 4095	1	2
4096 - 8191	1	4
8192 - 16383	1	8
16384 - 32767	1	16
32768 - 65535	1	32
65536 - 129023	1	63
129024 - 258047	2	63
258048 - 516095	4	63
516096 - 1032191	8	63
1032192 - 2064383	16	63
2064384 - 4128767	32	63

iv) Calculate the Niq = [Ntiqtemp/(Nc*Ncic)] that is required. [...] = next largest integer.

v) Also one must ensure the frequency band requested is within the physical limits available. These limits depend on the modulation function chosen and the requirement of the smallness of f at tp/2. Min Ntiq=Ntiqmn=2*512, Max Ntiq=Ntiqmx=63*2048*Ncmx. Ncmx is currently 32. The relationship between Ntiq and dw is dw*A*Ntiq*10*10^(-9)=a, therefore

dw_max = 10^(9) a / (10 A * 512 * 2) (in radians/sec),
dw_min=dw_max / (128 Ncmx)

dw must be constrained to be within this range.

for the ln-sech, A=.1 and a = 5 giving
dw_max=5*10^9/(512*2)rad/sec = 4882.5Krad/sec = 777KHz/sec
dw_min =5*10^9/(2048*63*Ncmx)rad/sec = 38.75/NcmxKrad/sec = 6.168/Ncmx KHz/sec

The order of the programming will not follow the order of the explanation .., but should follow the order of the example implementation for the ln-sec function in the previous section.