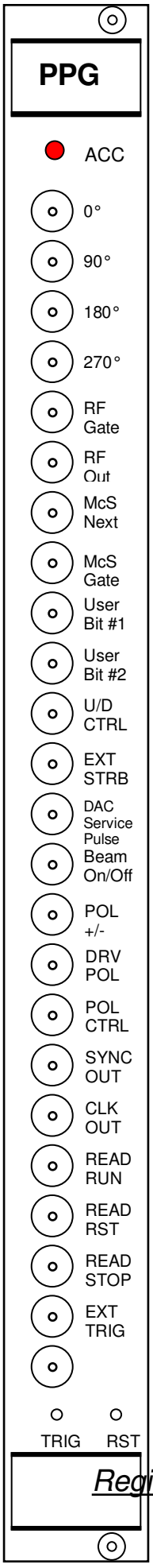


TRIUMF

VME Pulse Programmer Module

General Description

The VME Pulse Programmer (PPG) module was designed for use with SpinCore Technologies Inc. PulseBlaster®, an intelligent general purpose pulse/pattern generation board. Refer to the PulseBlaster owner's manual for programming instructions.

VME Interface SLAVE – A16, D8(OE)

The PPG requires a 16 bit address space. Jumpers on the printed circuit board configure the base address selection.

Address Modifier Selection

The PPG will only respond to A16 address cycles.
Short Supervisory & privileged access - 0x2D, 0x29

Base Address Selection

Each jumper corresponds to address bits A15 – A5 on the VME address bus. Installing a jumper for each address bit will select a 0 (low) for the corresponding VME address bit.

Jumpers Installed (X)											Address Range
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	
X	X	X	X	X	X	X	X	X	X	X	0000 – 001F
-	X	X	X	X	X	X	X	X	X	X	8000 – 801F
-	-	-	-	-	X	X	X	X	X	X	F800 – F81F
-	-	-	-	-	-	-	-	-	-	-	FFE0 – FFFF

Input/Output Description

PPG Interface output pins (J4 on the PCB) are TRUE HIGH TTL signals.

0°, 90°, 180°, 270°, RF Gate, RF Out, McS Next, McS Gate, User Bit #1, User Bit #2, U/D CTRL, EXT STRB, DAC Service Pulse, Beam On/Off, POL +/-, DRV POL, POL CTRL, SYNC OUT, READ RUN, READ RST, READ STOP, EXT TRIG and EXT RST signals are input NIM signals (-0.8 volts NIM = logic HIGH TTL).

DRV POL is an open collector output with maximum continuous current rating of 200 mA.

CLK OUT is a TTL clock signal from the PulseBlaster.

Register Description

The first 8 registers are used to control/program the PulseBlaster. Writing to register FFF0 is equivalent to writing to ISA port XXX+0 where XXX is the base address. Refer to the PulseBlaster owner's manual for more information.

Note: a read of any PulseBlaster control/program register will return a result of zero.

PulseBlaster Control Registers

Command 0 – Device Reset: XXX0 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX0 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 1 – Start Trigger: XXX1 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX1 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 2 – Load Number of Bytes per Word: XXX2 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX2 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 3 – Select Memory Device: XXX3 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX3 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 4 – Clear Address Counter: XXX4 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX4 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 5 – Not Used: XXX5 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX5 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 6 – Load Memory: XXX6 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX6 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Command 7 – Programming Finished: XXX7 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX7 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

VME Module Control Registers

Output Polarity Mask (High byte) Register: XXX8 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX0 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Output Polarity Mask (Middle byte) Register: XXX9 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXX9 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Output Polarity Mask (Low byte) Register: XXXA (Default: 80H)

This register will respond to a byte accesses only.

ADR	$XXXA (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	0	0	0

Select Ext/Int Polarization Source Control Register: XXXB (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXXB (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Bit1,Bit 0:
- 00B: VME control.
- 01B: External control.
- 10B: PulseBlaster control via CH15
- 11B: Not Used; polarity driver set high (ie. Pulled high)

VME Polarization Set Register: XXXC (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXXC (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R/W
RESET	0	0	0	0	0	0	0	0

Bit 0: Bit is clear (0): Polarity driver pulled high.
Bit is set (1): Polarity driver pulled to ground.

VME Read Status Register: XXXD (Default: XXH)

This register will respond to a byte accesses only.

ADR	$XXXD (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	X	X	X	X	X	X	X	X

Bit 0: Bit is clear (0): PulseBlaster is NOT reset.
Bit is set (1): PulseBlaster IS reset.

Bit 1: Bit is clear (0): PulseBlaster is NOT running.
Bit is set (1): PulseBlaster IS running.

Bit 2: Bit is clear (0): PulseBlaster is NOT stopped.
Bit is set (1): PulseBlaster IS stopped.

Bit 3: VME polarization source control bit 0.

Bit 4: VME polarization source control bit 1.

Bit 5: Bit is clear (0): VME polarization control off.
Bit is set (1): VME polarization control active.

Bit 6: Not used

Bit 7: Bit is clear (0): External polarization control off.
Bit is set (1): External polarization control active.

VME Trigger Register: XXXE (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXXE (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Write cycle will generate a 150ns Hi-Lo-Hi trigger pulse to the PulseBlaster.

VME Reset Register: XXXF (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XXXF (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Write cycle will generate a 150ns Hi-Lo-Hi reset pulse to the PulseBlaster.

VME Reset Counters Register: XX10 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX10 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Write cycle will generate a 150ns Hi-Lo-Hi reset pulse to the counter registers.

VME McS Counter (Byte 3) Register: XX11 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX11 (Bits 31-24)							
BIT	31	30	29	28	27	26	25	24
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME McS Counter (Byte 2) Register: XX12 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX12 (Bits 23-16)							
BIT	23	22	21	20	19	18	17	16
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME McS Counter (Byte 1) Register: XX13 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX13 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME McS Counter (Byte 0) Register: XX14 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX14 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	0	0	0	0	0	0	0

VME Cycle Counter (Byte 3) Register: XX15 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX15 (Bits 31-24)							
BIT	31	30	29	28	27	26	25	24
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME Cycle Counter (Byte 2) Register: XX16 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX16 (Bits 23-16)							
BIT	23	22	21	20	19	18	17	16
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME Cycle Counter (Byte 1) Register: XX17 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX17 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME Cycle Counter (Byte 0) Register: XX18 (Default: 00H)

This register will respond to a byte accesses only.

ADR	$XX18 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

VME Beam Control Register: XX19 (Default: 01H)

This register will respond to a byte accesses only.

ADR	$XX19 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R/W	R/W
RESET	0	0	0	0	0	0	0	1

Beam Off: Bit 0 is clear (0)
Bit 1 is clear (0)

Beam ON: Bit 0 is set (1)
Bit 1 is clear (0)

PPG control: Bit 0 is clear (0)
Bit 1 is set (1)

PPG control: Bit 0 is set (1)
Bit 1 is set (1)

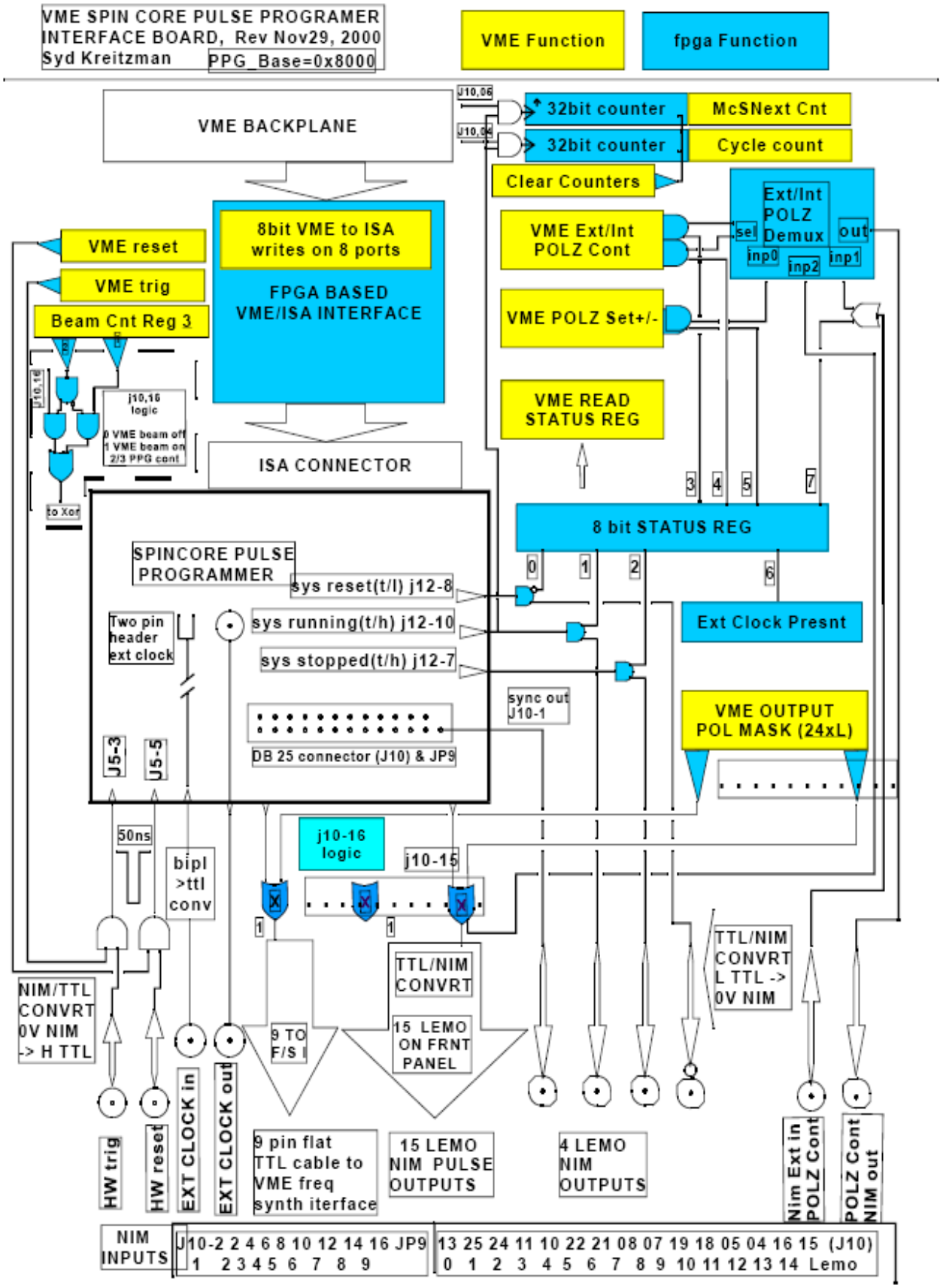
External Trigger Control Register: XX1A (Default: 01H)

This register will respond to a byte accesses only.

ADR	$XX19 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R/W
RESET	0	0	0	0	0	0	X	1

Bit 0: Bit is clear (0): External trigger is ENABLED.
Bit is set (1): External trigger is DISABLED.

Bit 1: Bit is clear (0): External trigger level in INACTIVE state.
Bit is set (1): External trigger level in ACTIVE state.


VME SPIN CORE PULSE PROGRAMER
INTERFACE BOARD, Rev Nov29, 2000
Syd Kreitzman
PPG_Base=0x8000
VME Function
fpga Function
VME BACKPLANE
32bit counter
McSNext Cnt
32bit counter
Cycle count
Clear Counters
Ext/Int POLZ Demux
sel
out
inp0
inp2
inp1
VME reset
VME trig
Beam Cnt Reg 3
8bit VME to ISA writes on 8 ports
FPGA BASED VME/ISA INTERFACE
VME Ext/Int POLZ Cont
VME POLZ Set+/-
VME READ STATUS REG
j10,16 logic
0 VME beam off
1 VME beam on
2/3 PPG cont
ISA CONNECTOR
to Xor
8 bit STATUS REG
SPINCORE PULSE PROGRAMMER
sys reset(t/l) j12-8
Two pin header ext clock
sys running(t/h) j12-10
sys stopped(t/h) j12-7
Ext Clock Presnt
sync out J10-1
VME OUTPUT POL MASK (24xL)
DB 25 connector (J10) & JP9
J5-3
J5-5
50ns
bipl >ttl conv
j10-16 logic
j10-15
TTL/NIM CONVRT
TTL/NIM CONVRT L TTL -> 0V NIM
NIM/TTL CONVRT 0V NIM -> H TTL
9 TO F/S I
15 LEMO ON FRNT PANEL
HW trig
HW reset
EXT CLOCK in
EXT CLOCK out
9 pin flat TTL cable to VME freq synth iterface
15 LEMO NIM PULSE OUTPUTS
4 LEMO NIM OUTPUTS
Nim Ext in POLZ Cont
POLZ Cont NIM out
NIM INPUTS
J10-2 2 4 6 8 10 12 14 16 JP9
1 2 3 4 5 6 7 8 9
13 25 24 11 10 22 21 08 07 19 18 05 04 16 15 (J10)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 Lemo