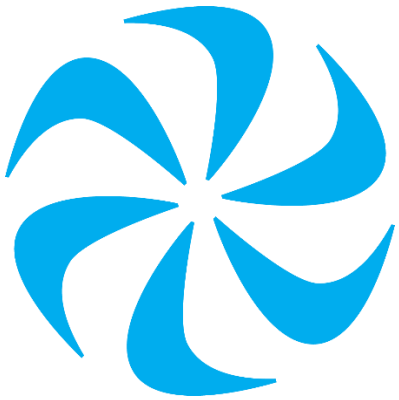
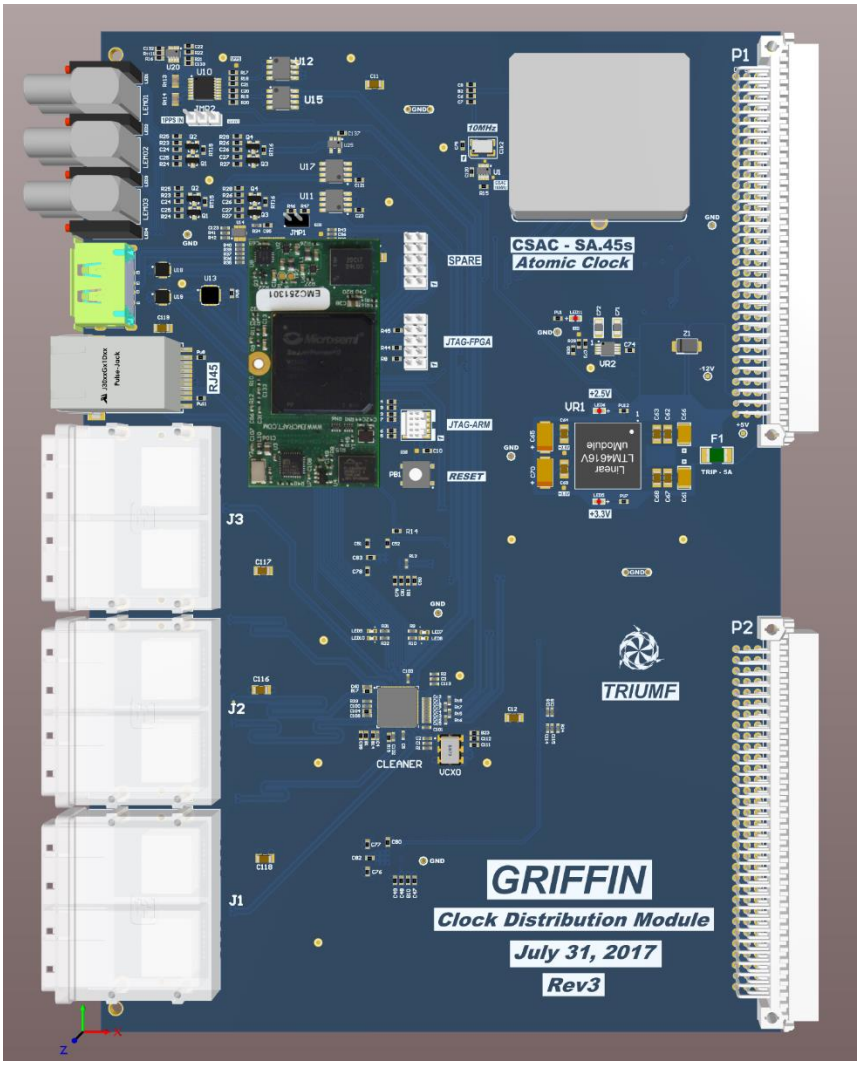


Clock Distribution Module
REV. 3

Contents

Overview



This document will briefly explain the operation and specification of the Clock Distribution Module (CDM), developed by the Electronics Development group at TRIUMF. The CDM provides a variety of input and outputs at both TTL and NIM logic levels to distribute a desired clock and trigger signal to multiple devices. The CDM has the ability to operate in a master/slave configuration to increase the number of outputs. In addition, the CDM has the ability to attach a CSAC-SA.45s Atomic Clock module to further reduce clock drift and add the ability to synchronize to a GPS clock

Once the module has been configured, it will retain its settings even after a loss of power event, allowing the module to automatically comeback on line in the appropriate configuration.

Quick-start

ESPER-tool is a python based communication script used to interface with the ESPER server running on the host device. The ESPER-tool will require the client machine to be running either Python V.2.7 or V.3.

Requirement

- Python version 2.7 or higher
- Internet access

Windows Installation

- Install Python
- On the client machine, install the ESPER-tool library using PIP. Open a command line window and type the following

```
C:\> pip install esper-tool
```

Linux Installation

```
# pip install esper-tool
```

Using Esper-Tool

- To begin using the ESPER-tool ensure that the host is running the server by visually inspecting the ESPER status led. Connect the client using the following command

```
esper-tool <host ip>
```

- Successful connection should result in the following command line prompt

```
Type 'help' for a list of available commands
[http://<host ip>:/system]>
```

- If the connection fails, verify the Ethernet port is active by reseating the Ethernet cable
- Commands can be displayed by typing "help" into the command line. Further details on the commands can be found by typing the command after help "help read"

```
[http://<host ip>:/system]> help

Documented commands (type help <topic>):
========================================
cd        exit  list  module  read    uptime   write
download  help  ls    quit    upload  version

[http://<host ip>:/system]> help read
Purpose: Read module variable(s)
Usage: read <vid> [offset] [length] [repeat]
```

Reading Variables

- To read all variables in a module type ***read*** within the module, to read a specific variable type ***read*** followed by the variable name

```
[http://192.168.50.200:/system]> read
vid   key                  type          options  status        data
---   ---                  ----          -------     ------     ----
0     device               ascii            R                 "Linux"
1     version              uint32           R                   [1]
2     debug_level          uint8            RW                  [2]
3     num_modules          uint32           R                   [5]

[http://192.168.50.200:/system]> read version
[1]
```

- If the variable is a string or an array, an <offset> and <length> argument will need to be added

```
[http://<host ip>:/system]> help read
Purpose: Read module variable(s)
Usage: read <vid> [offset] [length] [repeat]

[http://192.168.50.200:/system]> read device 0 4
Linu
[http://192.168.50.200:/system]> read device 0 5
Linux
```

Writing Variables

- Variables can only be written to one at a time, except for the case of array, which can be sent an entire array of data. Similarly to read an offset can be applied to arrays to write specific values

```
[http://192.168.50.200:/mod_cdm]> write source_sel true
[http://192.168.50.200:/mod_cdm]> write sel_nim 0
[http://192.168.50.200:/mod_cdm]> write source_sel true
[http://192.168.50.200:/mod_lmk]> write dclkoutx_div [30,30,30,30,30,30,30]
[http://192.168.50.200:/mod_lmk]> write dclkoutx_div 2 30
```

Specifications

Signals

Inputs	Connectors	Level
External CLK	00 – LEMO 50Ω Female Socket	TTL / NIM
External TRG		
ESATA TRG	eSATA	TTL
ESATA CLK		

Outputs		
CLK	MiniSAS -> eSATA	LVDS
TRG		
Manual TRG		
10Mhz	00 – LEMO 50Ω Female Socket	NIM
1 Pulse Per Second		
CLK 7		
Multi TRG		
CLK 6	VME Bus P1 B21	TTL

Electrical

Symbol	Input	Output DC	Output AC	Switching Frequency
VR1A	+5V	+3.3V	$12mV_{P-P}$	1.25MHz
VR1B		+2.5V		
VR2	-12V	-3.3V	$17.5uV_{RMS}$	NA

Reference Clock

Communication

Serial
Ethernet

Mechanical

Board Dimensions: 163mm x 233mm (WxH)
Back Plane Connectors:

Hardware

FPGA

The FPGA module used on the CDM is a M2S-FG484 Microsemi SmartFusion2 running an embedded version of Linux, which runs the ESPER server allowing the user to modify module parameters.

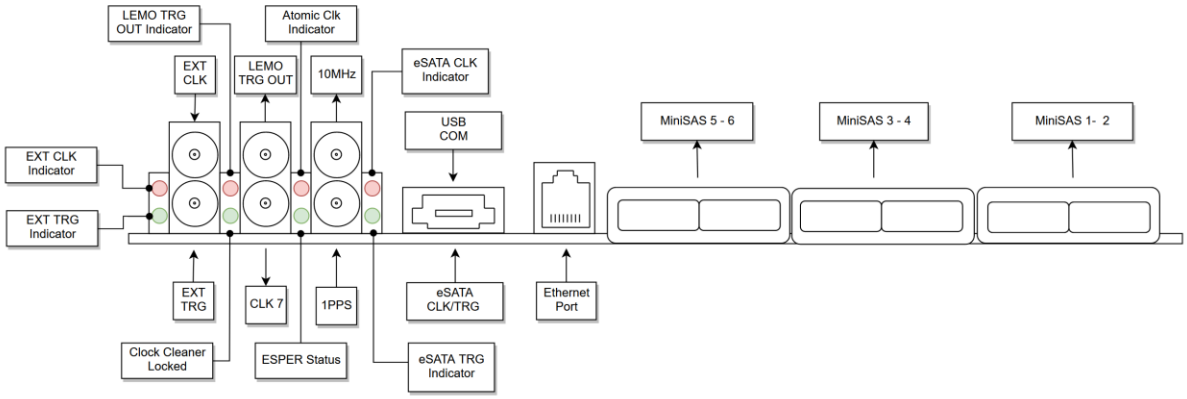
Clock Cleaner

The core of the CDM is the *LMK04821Low Noise Clock Jitter Cleaner*

Atomic Clock

In the event a more precise reference clock is needed, the CMD module has the capability to use a CS

Front Panel



The front panel of has a variety of inputs, outputs, communication ports and LED indicators

Name	Category	Direction	Description
EXT CLK	Clock Signal	Input	The external clock signal fed though 00 Lemo connector, signal level can be either NIM or TTL. This signal can be used as the clock cleaners reference if configured, and can be monitors though thought the *ext_clk* variable in the CDM ESPER module
EXT TRG	Trigger Signal	Input	The external Trigger signal fed though 00 Lemo connector, signal level can be either NIM or TTL. This Trigger can be fanned out to the miniSAS connectors if configured, and can be monitored thought the *ext_trg* variable in the CDM ESPER module

Manual TRG*	Trigger Signal	Output	The Manual trigger is a user defined trigger signal that can be triggered by writing any value top the ***man_sync*** variable in the CMD ESPER module. The number assigned to this variable controls the duration, see appendix for more details *If needed the Atomic clock can be synchronized to a GPS 1PPS signal
CLK 7	Clock Signal	Output	Clock Signal 7 is a clock fed directly from the LMK04821 clock cleaner
10MHz	Clock Signal	Output	The 10MHz signal is a fed by either the onboard 10MHz crystal oscillator or the Atomic clock if configured. **see Clock Flow Diagram**
1PPS	Trigger Signal	Output	The Atomic clock can be configured to output a 1 pulse per second
eSATA CLK/TRG	Clock/Trigger Signal	Input	The eSATA port can be used to provide the
Ethernet Port	Communication	Bi-Directional	To communicate with the ESPER server the CDM will need to be connected to a network that the client can access
MiniSAS 1 - 6	Clock/Trigger Signal	Output	The miniSAS ports will carry both the clock (x4) and trigger (x4) signals
EXT CLK Indicator	Indicator	NA	The external clock indicator will illuminate if there is a clock signal applied to the EXT CLK port
EXT TRG Indicator	Indicator	NA	The external trigger indicator will illuminate if it is being routed to the miniSAS trigger outputs. The indicator will blink when a trigger is received
eSATA CLK indicator	Indicator	NA	The eSATA clock indicator will blink if a clock needs to be applied to it. The indicator will go solid when the internal PLL locks
eSATA TRG indicator	indicator	NA	The eSATA trigger indicator will illuminate if it is being routed to the miniSAS trigger outputs. The indicator will blink when a trigger is received
Atomic CLK indicator	indicator	NA	If an atomic clock is installed at start up the indicator will blink, when the indicator goes solid the clock is locked.
ESPER Status	Indicator	NA	Blinking indicates the ESPER server is up and running

Clock Flow Diagram

The CDM module can output 26 clocks without the need for an external reference clock, one Lemo connector outputs a fixed 10MHz signal from the onboard oscillator, and the other Lemo outputs the LMK output clock; both signals are NIM. Six miniSAS connectors output 24 LVDS clocks that can be individually disabled to reduce power consumption.

The LMK clock cleaner can accept an alternative references clock through the Lemo or eSATA connector. To use an alternative reference clock refer to the lmk04821 documentation for appropriate settings.

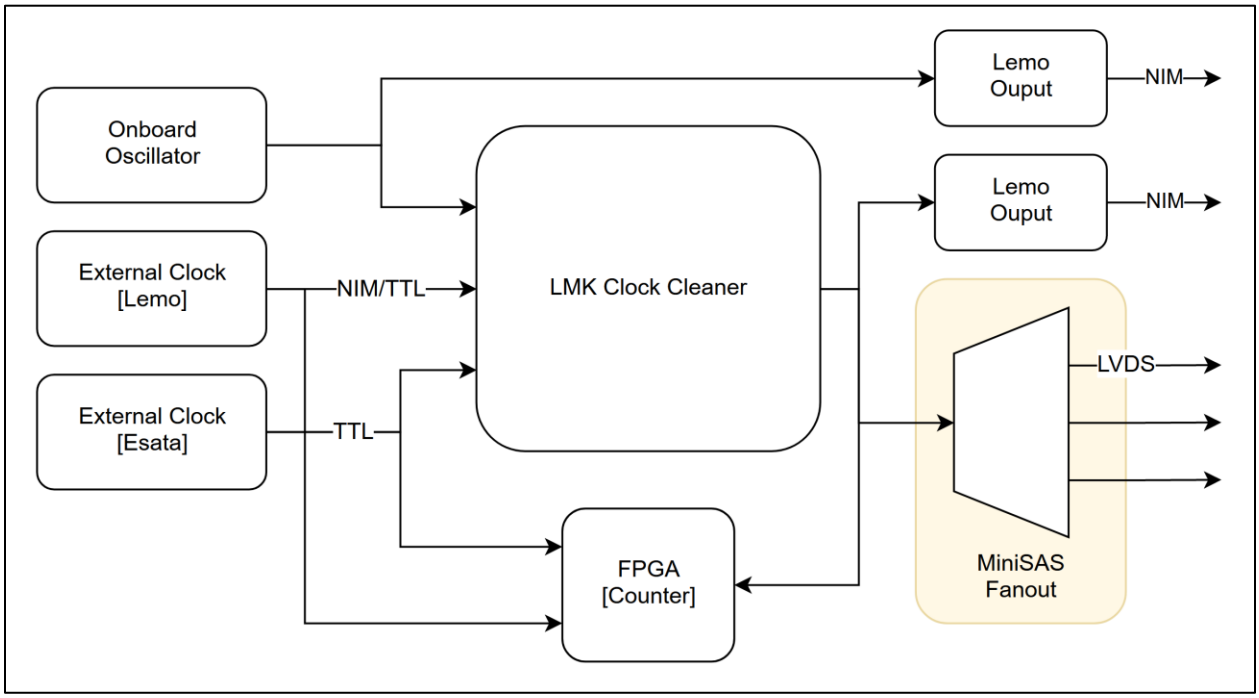


Figure 1 Top Level Clock Diagram

The CDM comes with a standard 10MHz onboard oscillator, but has the capability to install an atomic clock module, for greater precision. To switch between the two, the “atomic_clk_sel” variable in the CDM module needs to be adjusted. When an Atomic clock is installed with a valid id to the CDM during the power up phase, the CDM module will automatically select the atomic clock as its onboard reference.

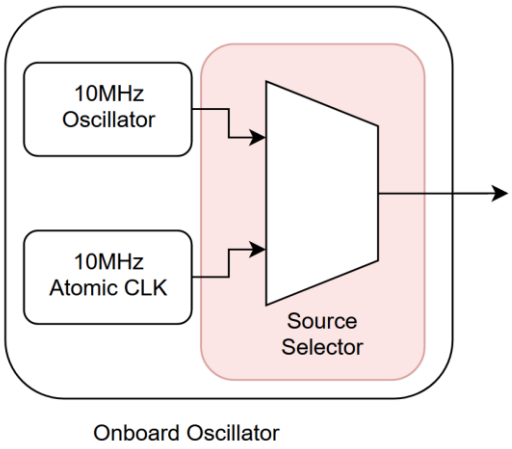


Figure 2 Onboard Oscillator Diagram

Trigger Flow Diagram

From the top level, the CDM can take in two triggers and output up to two triggers simultaneously. The input triggers can be provided through either the Lemo connectors or the eSATA connector. The Lemo trigger input can accept a NIM or TTL signal, while the eSATA trigger must be TTL.

The trigger can be output through the external output Lemo connector, or through the miniSAS connectors. The output Lemo trigger is synchronized to the output clock, and output at the NIM signal level. The miniSAS trigger output could be synchronized or unsynchronized by setting the "sas_trg_sync" variable in the CDM module to 1 or 0 respectively, the signal from the miniSAS connector is at LVDS

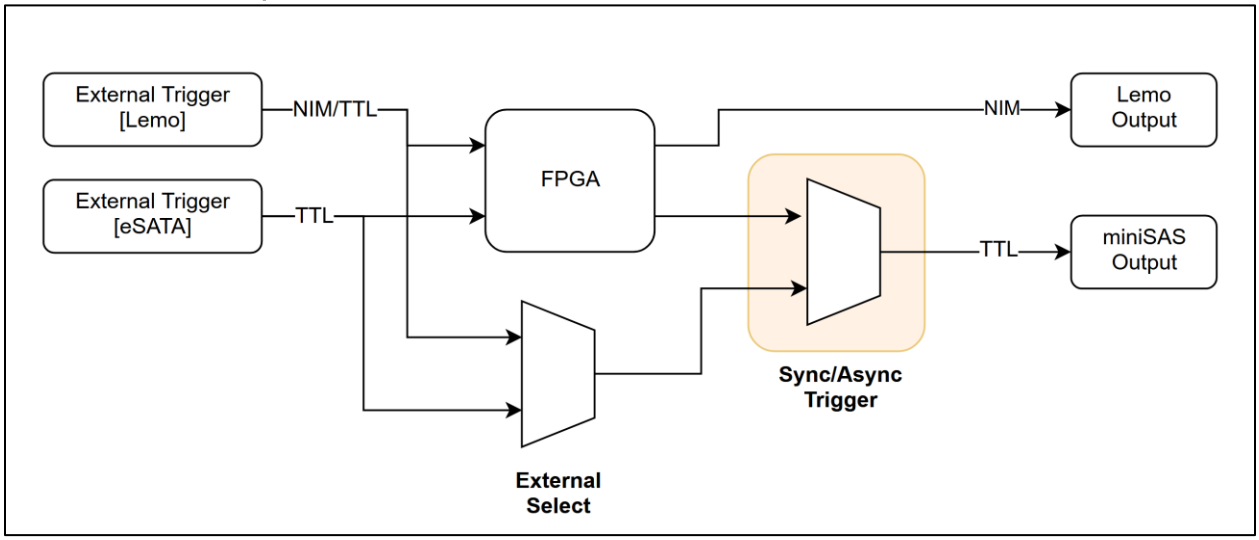


Figure 3 Top Level Trigger Diagram

Looking into the FPGA trigger circuit shows five possible trigger blocks, which can be individually routed to the Lemo or miniSAS connector. The “lemo_trg_sel” and the “sas_trg_sel” variables in the CDM module control the trigger output to the Lemo and miniSAS respectively.

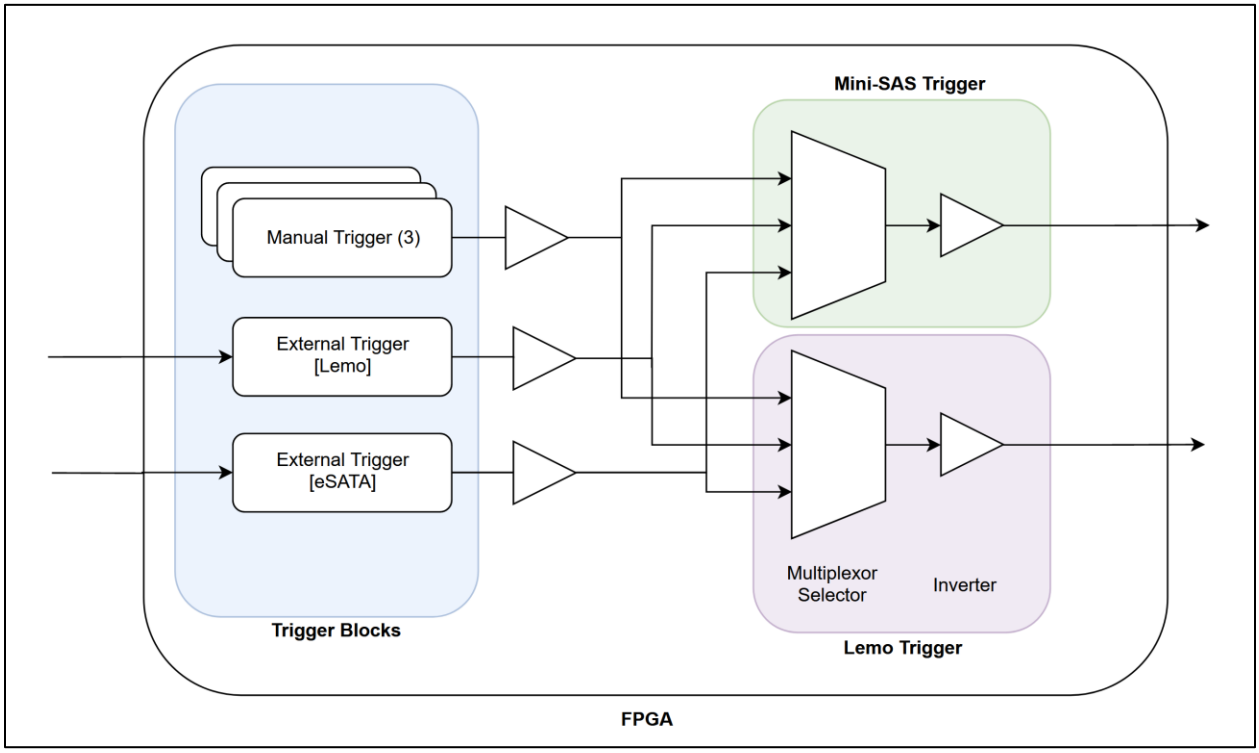


Figure 4 FPGA Trigger Diagram

Each CDM trigger source is made up of a trigger block that allows the user to customize either the externally provided trigger or the internal user defined trigger. The external triggers can be inverted and applied to a one-shot controller, with an adjustable duration measured in clock cleaner clock cycles. The user defined manual trigger has the same capability mentioned above, with the additional feature of being able to implement a periodic trigger.

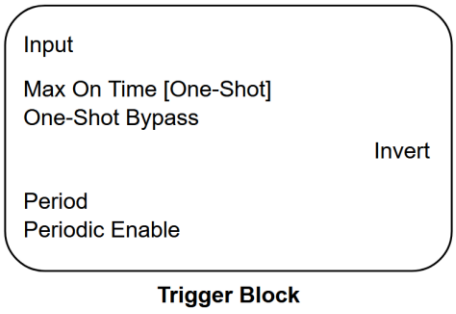


Figure 5 Trigger Block Diagram

Software

ESPER Modules

The CDM is running a user interface server that will allow an operator to configure the module to meet the desired synchronization needs.

Firmware Update

- Pull repository
- Open Libero 11.8 SP3
    - Update eNVM content with u-boot.hex inside “emcraft_firmware” directory
    - Program board
- Copy “cdm.Uimage” to the host TFTP server
- Connect to board through Putty
- If Linux terminal comes up reboot the system with “reboot –f”
- Press any key when the u-boot terminal comes up
- Erase current u-boot environment variables
    - Use “sf probe 0” to connect with the spi flash
    - Use “sf erase 0 100” to erase the current environment variables
    - Use “reset” and press any key again to enter u-boot
    - Should see” Warning –bad CRC using default environment”
- Update Linux image
    - Set server IP to the IP of the TFTP server that has the Linux image, using “setenv server <ip>”
    - Use “run update” to flash the Linux image
- Use “saveenv” to save current environment variables
- Reset board

Building Image

- Pull repository
- Run “insall.sh” from fw directory
- Run “ACTIVATE.sh” from linux-cortexm-1.14.3/ directory
- Run “make” from linux-cortexm-1.14.3/projects/cdm/ directory
- This will create a bootable image “cdm.Uimage”

Appendix

CDM Module

Variable Name	Description	Default	GRIFFIN Master	GRIFFIN Slave	ALPHA Master	ALPHA Slave
Sel_nim	Select the trigger and clock input level for the lemo input		1			
Sel_atomic_clk	On board 10MHz clock selector 0 : Onboard 10MHz Oscillator 1 : Optional 10MHz atomic clock		0			
Sel_ext	Hardware trigger select 0 : eSATA 1: Lemo		1			
Clkx_y_en	MiniSAS x output enable 0 : Output disabled 1: Output enabled		1			
Sas_trg_sync	Select hardware or digitized trigger signal 0 : Asynchronous hardware trigger 1: Synchronous digitized trigger		1			
Esata_trg	eSATA trigger count		Na			
Esata_os_bybass	eSATA trigger one-shot bypass, output to MiniSAS 0 : Enable one-shot circuit 1 : Disable one-shot circuit					
Esata_invert	eSATA trigger invert, output to MiniSAS 0 : Normal output 1: Invert output					
Esata_max_on	eSATA one-shot maximum on time, , output to MiniSAS					
Ext_trg	External trigger count					
Ext_os_bypass	External trigger one-shot bypass, output to MiniSAS 0 : Enable one-shot circuit 1 : Disable one-shot circuit					
Ext_invert	External trigger invert, output to MiniSAS 0 : Normal output 1: Invert output					
Ext_max_on	External one-shot maximum on time, , output to MiniSAS					
Man_trg_x	User defined trigger (3) level 0 : Output low 1: Output high					
Man_os_bypass_x	User defiend trigger (3) one-shot bypass 0 : Enable one-shot circuit 1 : Disable one-shot circuit					
Man_invert_x	User defined trigger (3) invert output 0 : Normal output 1: Invert output					
Man_max_on_x	User defined trigger (3) one-shot max on time in clock cleaner clock cycles					
Man_period_x	User defined trigger (3) period					
Man_period_en_x	User defined trigger (3) periodic output enable 0 : Disable periodic circuity 1 : Enable periodic circuity					
Lemo_trg_sel	Lemo trigger output source 0: eSATA					

	1: External 2: Manual Trigger 0 3: Manual Trigger 1 4: Manual Trigger 2					
Lemo_invert	Lemo trigger invert 0 : Normal 1: Invert output					
Sas_trg_sel	MiniSAS trigger output source 0: eSATA 1: External 2: Manual Trigger 0 3: Manual Trigger 1 4: Manual Trigger 2					
Sas_invert	MiniSAS trigger invert 0 : Normal 1: Invert output					
Esata_freq	eSATA input frequency					
External_ref	External input frequency					
Cc_freq	Clock clean frequency					

LMK Module

Variable Name	Description	Default	GRIFFIN Master	GRIFFIN Slave	ALPHA Master	ALPHA Slave
OSCout_MUX	Source of OSCout 0: Buffered OSCin	0	0	0	0	0
OSCout_FMT	Output format of OSCout 1: Power down (CLKin2) 4: LVPECL 2000mVpp	4	1	1	1	0
VCO_MUX	Clock distribution path source from VCO0, VCO1, or CLKin 0: VCO0 1: VCO1	0	1	1	1	1
SYSREF_CLKin0_MUX	SYSREF output from SYSREF_MUX or CLKin0 0: SYSREF_MUX	0	0	0	0	0
SYSREF_MUX	SYSREF source 0: Normal Sync	0	0	0	0	0
SYSREF_DIV	Divide value for SYSREF output	3072	3072	3072	3072	3072
SYSREF_DDLY	Digital delay value for SYSREF	8	8	8	8	8
SYSREF_PULSE_CNT	Number of SYSREF pulses generated when not in continuous mode	3	3	3	3	3
PLL2_NCLK_MUX	Select input to PLL2 N Divider 0: PLL prescaler	0	0	0	0	0
PLL1_NCLK_MUX	Select input to PLL1 N Divider 0: OSCin 1: Feedback mux	0	0	1	0	1
FB_MUX	Clock output fed into PLL1 N divider when in 0-delay mode 0: DCLKout6	0	0	0	0	0
FB_MUX_EN	Must be set to 1 when in 0-delay mode to enable mux 0: Feedback Mux powered down 1: Feedback Mux enabled	0	0	1	0	1
PLL1_PD	Power down PLL1 0: Normal operation	0	0	0	0	0
VCO_LDO_PD	Power down VCO_LDO	0	0	0	0	0

	0: Normal operation					
VCO_PD	Power down VCO 0: Normal operation	0	0	0	0	0
OSCin_PD	Power down OSCin port 0: Normal operation	0	0	0	0	0
SYSREF_GBL_PD	Power down individual SYSREF outputs depending on SDCLKoutY_DIS_MODE 0: Normal Operation 1: Active power down mode	0	1	1	1	1
SYSREF_PD	Power down SYSREF and divider 1: Power down	1	1	1	1	1
SYSREF_DDLY_PD	Power down SYSREF digital delay circuitry 1: Power down	1	1	1	1	1
SYSREF_PLSR_PD	Power down SYSREF pulse generator 1: Power down	1	1	1	1	1
DDLYd_SYSREF_EN	Enable digital delay on SYSREF output 0: Disable	0	0	0	0	0
DDLYd12_EN	Enable digital delay on DCLKout12 output 0: Disable	0	0	0	0	0
DDLYd10_EN	Enable digital delay on DCLKout10 output 0: Disable	0	0	0	0	0
DDLYd8_EN	Enable digital delay on DCLKout8 output 0: Disable	0	0	0	0	0
DDLYd6_EN	Enable digital delay on DCLKout6 output 0: Disable	0	0	0	0	0
DDLYd4_EN	Enable digital delay on DCLKout4 output 0: Disable	0	0	0	0	0
DDLYd2_EN	Enable digital delay on DCLKout2 output 0: Disable	0	0	0	0	0
DDLYd0_EN	Enable digital delay on DCLKout0 output 0: Disable	0	0	0	0	0
DDLYd_STEP_CNT	Number of dynamic digital delay adjustment 0: No adjustment	0	0	0	0	0
SYSREF_CLR	Except during SYSREF setup this bit should be set to 0	1	0	1		
SYNC_1SHOT_EN	SYNC one shot enables edge sensitive SYNC 0: SYNC is level sensitive, output will be held as long as SYNC is asserted	0	0	0	0	0
SYNC_POL	Set polarity of SYNC pin 0: Normal 1: Inverted	0	1	1	1	1
SYNC_EN	Enable SYNC functionality 1: Enabled	1	1	1	1	1
SYNC_PLL2_DLD	0: Off	0	0	0	0	0
SYNC_PLL1_DLD	0: Off	0	0	0	0	0
SYNC_MODE	Select method of generating a SYNC event 1: From SYNC pin or if enabled the DLD flags	1	1	1	1	1
SYNC_DISSYSREF	Prevents SYSREF clocks from becoming synchronized during SYNC events	0	0	0	0	0
SYNC_DIS12	Prevents device clock outputs from becoming synchronized during SYNC event	0	0	0	0	0
SYNC_DIS10	Prevents device clock outputs from becoming synchronized during SYNC	0	0	0	0	0
SYNC_DIS8	Prevents device clock outputs from becoming synchronized during SYNC	0	0	0	0	0
SYNC_DIS6	Prevents device clock outputs from becoming synchronized during SYNC	0	0	0	0	0
SYNC_DIS4	Prevents device clock outputs from becoming synchronized during SYNC	0	0	0	0	0

SYNC_DIS2	Prevents device clock outputs from becoming synchronized during SYNC	0	0	0	0	0
SYNC_DIS0	Prevents device clock outputs from becoming synchronized during SYNC	0	0	0	0	0
CLKin2_EN	Enable CLKin2 during auto-switch mode 0: Not enabled for auto-switch	0	0	0	0	0
CLKin1_EN	Enable CLKin2 during auto-switch mode 1: Enabled for auto-switch	1	1	1	1	1
CLKin0_EN	Enable CLKin2 during auto-switch mode 1: Enabled for auto-switch	1	1	1	1	1
CLKin2_TYPE	CLKin2 input type 0:Bipolar	0	0	0	0	0
CLKin1_TYPE	CLKin1 input type 0:Bipolar	0	0	0	0	0
CLKin0_TYPE	CLKin0 input type 0:Bipolar	0	0	0	0	0
CLKin_SEL_POL	Invert CLKin polarity used in pin select mode 0: Active high	0	0	0	0	0
CLKin_SEL_MODE	Sets the mode used in determining the reference for PLL1 0: CLKin0 Mannual 1: CLKin1 Manual 3: Pin select mode	3	0	1	0	1
CLKin1_OUT_MUX	Select where the output of the CLKin1 buffer is directed 2: PLL1	2	2	2	2	2
CLKin0_OUT_MUX	Select where the output off the CLKin0 buffer is directed 2:PLL1	2	2	2	2	2
CLKin_SEL0_MUX	Set the output value of the CLKin_SEL0 pin 0: Logic low	0	0	0	0	0
CLKin_SEL0_TYPE	Set the IO type of the CLKin_SEL0 pin 2: Input /w pull-up resistor	2	2	2	2	2
SDIO_RDBK_TYPE	Sets SDIO pin to open drain when SPI in 3wire read back mode 1: Output, open-drain	1	1	1	1	1
CLKin_SEL1_MUX	Sets the output value of CLKin_SEL1 pin 0: Logic low	0	0	0	0	0
CLKin_SEL1_TYPE	Sets the IO type of CLKin_SEL1 pin 2: Input /w pull-down resistor	2	2	2	2	2
RESET_MUX	Sets the output value of the RESET pin 0:Login low 6:SPI read back	0	6	6	6	6
RESET_TYPE	Sets the IO type of the RESET pin 2: Input /w pull-down resistor 3: Output push-pull	2	3	3	3	3
LOS_TIMEOUT	Time in which no activity on a CLKin forces a clock switch event 0: 370kHz	0	0	0	0	0
LOS_EN	Enable the Loss of signal timeout control 0: Disable	0	0	0	0	0
TRACK_EN	Enable the DAC to track PLL1 tuning voltage 1:Enabled, tracks when PLL1 locks	1	1	1	1	1
HOLDOVER_FORCE	Force holdover mode 0: Disabled	0	0	0	0	0
MAN_DAC_EN	Enable manual DAC mode 1:Manual	1	1	1	1	1
MAN_DAC	Sets the value of the DAC in holdover mode when used manually	512	512	512	512	512

DAC_TRIP_LOW	Voltage from ground at which hold over is entered 0: 1*Vcc/64	0	0	0	0	0
DAC_CLK_MULT	Multiplier for the DAC_CLK_CNTR which sets rate DAC value is traced 0: 4	0	0	0	0	0
DAC_TRIP_HIGH	Voltage from Vcc at which holdover is entered 0: 1*Vcc/64	0	0	0	0	0
DAC_CLK_CNTR	This with DAC_CLK_MULT sets rate at which the DAC is updated	127	127	127	127	127
CLKin_OVERRIDE	When CLKin_SEL_MODE = 0/1/2 CLKin_OVERRIDE will force the clock input 0: Normal, no overide	0	0	0	0	0
HOLDOVER_PLL1_DET	Enabled holdover when PLL1 lock transitions from high to low 0: Does not cause clock switch even	0	0	0	0	0
HOLDOVER_LOS_DET	Enabled holdover when PLL1 LOS is detected 0: Disabled	0	0	0	0	0
HOLDOVER_VTUNE_DET	Enabled DAC Vtune rail detection 0: Disabled	0	0	0	0	0
HOLDOVER_HITLESS_SWITCH	Determines whether a clock switch event will enter holdover using hitless switching 1: Hitless switching	1	1	1	1	1
HOLDOVER_EN	Holdover active 1: Enabled	1	1	1	1	0
HOLDOVER_DLD_CNT	Number of valid clocks of PLL1 PDF before holdover is exited	512	512	512	512	
CLKin0_R	Value of PLL1 N counter when CLKin0 selected	120	1	1	1	1
CLKin1_R	Value of PLL1 N counter when CLKin1 selected	150	100	10	10	10
CLKin2_R	Value of PLL1 N counter when CLKin2 selected	150	100	5	1	10
PLL1_N	N divider value for PLL1	120	10	5	10	10
PLL1_WND_SIZE	Window size used for digital lock detector for PLL1 3: 43ns	3	3	3	3	3
PLL1_CP_TRI	PLL1 charge pump output between active and tri-state 0 : PLL1 CPout is active	0	0	0	0	0
PLL1_CP_POL	PLL1 charge pump polarity 1: Positive Slope VCO/VCXO	1	1	1	1	1
PLL1_CP_GAIN	PLL1 charge pump output current 4: 450uA	4	4	4	4	4
PLL1_DLD_CNT	PLL1 digital lock detector counter	8192	8192	8192	8192	8192
PLL1_R_DLY	Cause output to lag CLKinX in 0-delay mode 0: 0ps	0	0	0	0	0
PLL1_N_DLY	Cause output to lead CLKinC in 0-delay mode 0:0ps	0	0	0	0	0
PLL1_LD_MUX	Set the output value of the Status_LD1 pin 1: PLL1 DLD	1	1	1	1	1
PLL1_LD_TPYE	Set the IO type of the Status_LD1 pin 6: Output Open Drain	6	6	6	6	6
PLL2_R	PLL2 R divider Value	2	64	32	64	64
PLL2_P	PLL2 N pre-scalar divides the output of VCO selected by Mode_MUX1	2	8	8	8	8
OSCin_FREQ	The frequency of the PLL2 reference input to the PLL2 phase detector 0: 0 to 63MHz 1: 63MHz – 127<MHz	7	1	1	1	1

	7: Reserved					
PLL2_XTAL_EN	Amplifier for external crystal oscillator used for PLL2 0: Amplifier disabled	0	0	0	0	0
PLL2_REF_2x_EN	Double the frequency applied to PLL2 normally given by the VCXO 1: Doubler Enabled	1	1	1	1	1
PLL2_N_CAL	PLL2 N calibration Value	12	60	30	80	60
PLL2_FCAL_DIS	Disabled PLL2 frequency calibration 0: frequency calibration enabled	0	0	0	0	0
PLL2_N	PLL2 N divider value	12	60	30	80	60
PLL2_WND_SIZE	Window size used for digital lock detector for PLL2 2: 3.7ns	2	2	2	2	2
PLL2_CP_GAIN	PLL2 charge pump output current 3: 3200uA	3	3	3	3	3
PLL2_CP_POL	PLL2 charge pump polarity 0: Negative slope VCO/VCXO	0	0	0	0	0
PLL2_CP_TRI	PLL2 charge pump output between active and tri-state 0: Output Disabled	0	0	0	0	0
SYSREF_REQ_EN	Enabled SYNC/SYSREF_REQ pin to force SYSREF_MUX = 3 for continuous pulse	0	0	0	0	0
PLL2_DLD_CNT	PLL2 digital lock detect counter	8192	8192	8192	8192	8192
PLL2_LF_R4	Internal loop filter component 0: 200Ω	0	0	0	0	0
PLL2_LF_R3	Internal loop filter component 0: 200Ω	0	0	0	0	0
PLL2_LF_C4	Internal loop filter component 0: 10pF	0	0	0	0	0
PLL2_LF_C3	Internal loop filter component 0: 10pF	0	0	0	0	0
PLL2_LD_MUX	Sets the output value for the Stauts_LD2 pin 2: PLL2 DLD	2	2	2	2	2
PLL2_LD_TYPE	Sets the IO type of the Status_LD2 pin 3: Output Push-Pull 6: Output open drain	6	3	3	3	3
PLL2_PRE_PD	Power down PLL2 Pre-scalar 0: Normal operation	0	0	0	0	0
PLL2_PD	Power down PLL2 0: Normal Operation	0	0	0	0	0
VCO1_DIV	VCO1 divisor value 0: divide by 2	0	0	0	0	0
OPT_REG_1	Optimization register 21: LMK04821	21	21	21	21	21
OPT_REG_2	Optimization register 51: LMK04821	51	51	51	51	51
RB_PLL1_LD_LOST	Set to true when detecting a PLL1 DLD falling edge	NA	NA	NA	NA	NA
RB_PLL1_LD	PLL1 DLD status	NA	NA	NA	NA	NA
CLR_PLL1_LD_LOST	Reset the RB_PLL1_LD_LOST signal, will not clear the status when RB_PLL1_LD is low	NA	NA	NA	NA	NA
RB_PLL2_LD_LOST	Set to true when detecting a PLL2 DLD falling edge	NA	NA	NA	NA	NA
RB_PLL2_LD	PLL2 DLD status	NA	NA	NA	NA	NA
CLR_PLL2_LD_LOST	Reset the RB_PLL2_LD_LOST signal, will not clear the status when RB_PLL2_LD is low	NA	NA	NA	NA	NA
RB_DAC_VALUE	Holdover DAC value	NA	NA	NA	NA	NA
RB_CLKin2_SEL	PLL1 clkin selection	NA	NA	NA	NA	NA

RB_CLKin1_SEL	PLL1 clkin selection	NA	NA	NA	NA	NA
RB_CLKin0_SEL	PLL1 clkin selection	NA	NA	NA	NA	NA
RB_CLKin1_LOS	CLKin1 loss of signal	NA	NA	NA	NA	NA
RB_CLKin0_LOS	CLKin0 loss of signal	NA	NA	NA	NA	NA
RB_HOLDOVER	Holdover active	NA	NA	NA	NA	NA
CLKoutX_Y_ODL	Output drive level	0	0	0	0	0
CLKoutX_Y_IDL	Input drive level	0	0	0	0	0
DCLKoutX_DIV	Division value of VCO	0	30	30	24	24
DCLKoutX_DDLY_CNTH	Number of clock cycles the output will be high when digital delay is active	5	5	5	5	5
DCLKoutX_DDLY_CNTL	Number of clock cycles the output will be low when the digital delay is active	5	5	5	5	5
DCLKoutX_ADLY	Device clock analog delay value	0	0	0	0	0
DCLKout_ADLY_MUX	Selects the input for the analog delay for device clock 0: Device clock output	0	0	0	0	0
DCLKoutX_MUX	Selects input to the device clock buffer 0: Divider only 3:Analog delay and divider	0	0	0	0	0
DCLKoutX_HS	Sets device clock half step value, half step must be 0 for divide of 1	0	0	0	0	0
SDCLKoutY_MUX	Sets the input to the SDCLKoutX output	0	0	0	0	0
SDCLKoutY_DDLY	Sets the number of VCO cycles to delay the SDCLKoutX by	0	0	0	0	0
SDCLKoutY_HS	Sets the SYSREF clock half step value	0	0	0	0	0
SDCLKoutY_ADLY_EN	Enable analog delay for the SYSREF output	0	0	0	0	0
SDCLKoutY_ADLY	Sets the analog delay value for SYSREF output	0	0	0	0	0
DCLKoutX_DDLY_PD	Power down digital delay circuity 0: Enabled 1: Power down	0	1	1	1	1
DCLKoutX_HSg_PD	Power down device clock glitch less half step 0: Enabled 1: Power down	1	1	1	1	1
DCLKoutX_ADLYg_PD	Power down device clock glitch less analog delay 0: Enabled 1: Power down	1	1	1	1	1
DCLKoutX_ADLY_PD	Power down analog delay circuitry 0: Enabled 1: Power down	1	1	1	1	1
CLKoutX_Y_PD	Power down clock groups 0: Enabled	0	0	0	0	0
SDCLKoutY_DIS_MODE	Configure the output state of SYSREF 0: Active in normal mode	0	0	0	0	0
SDCLKoutY_PD	Power down SDCLKoutY and set the state defined by SDCLKoutY_DIS_MODE 0: Enabled 1: Power down	1	0	0	0	0
SDCLKoutY_POL	Set the polarity of the clock on the eSDCLKoutY when device clock output is selected with SDCLKoutY_MUX 0: Normal	0	0	0	0	0
SDCLKoutY_FMT	Set the output format to the SYSREF clocks 0: Power down 1: LVDS	0	1	1	1	1
DCLKoutX_POL	Sets the polarity of the device clocks from the DCLKoutX outputs 0: Normal	0	0	0	0	0
DCLKoutX_FMT	Sets the output format of the device clocks	1	1	1	1	1

	0: Power Down 1: LDVS					

Template Module

Current Setup		Description
0	Custom	If any variable has changed by an ESPER write command the current setup variable will be set to custom
1	GRIFFIN Master	The GRIFFIN Master configure is set up to output a 50MHz clock signal while accepting its trigger signal thought the external LEMO connector and using the 10MHz Atomic clock as the reference clock for the clock cleaner.
2	GRIFFIN Slave	The GRIFFIN Slave configuration is set up to output a 50MHz clock signal while accepting the trigger signal though the eSATA connector and using the eSATA clock from the master as the reference clock for the clock cleaner.
3	ALPHA Master	The ALPHA Master Configure is set up to output a 62.5MHz clock signal while accepting the trigger signal though the eSATA connector and using external 10MHz clock input from CERN as the reference clock for the clock cleaner.
4	ALPHA Slave	The ALPHA Slave configuration is set up to output a 62.5MHz clock signal while accepting the trigger signal through the eSATA connector and using the eSATA clock from the master as the reference clock for the clock cleaner.