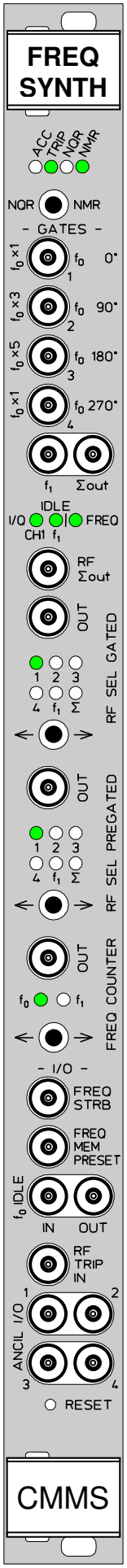

TRIUMF

β-NMR/β-NQR VME FREQ SYNTH Module

General Description

The VME FREQ SYNTH Module (VFS) was designed to generate a complex modulated swept signal summed with a reference frequency. The swept signal may be a single modulated carrier or include the modulated 3rd and 5th harmonics. Each carrier is independently modulated.

The carriers are synthesized and modulated digitally. The modulation data consists of up to 2048 I,Q pairs sampled at a submultiple of the carrier sample rate. The synthesizer circuit interpolates the I,Q sample rate to match the carrier sample rate before modulation.

VME Interface

SLAVE – A24, D32, D16, D8 (OE)

The VFS resides in 24-bit address space. Selector switches on the printed circuit board configure the base address. The front panel ACC led will indicate a successful VME access to the module.

Supported data transfers:

- D8(EO)
- D16 (aligned only)
- D32
- Read modify write
- D32 block mode

Address Modifier Selection

The VFS will only respond to A24 address cycles. The AM-SEL led will indicate a valid address modifier.

Supervisory & non-privileged access – 0x39, 0x3A, 0x3B, 0x3D, 0x3E, 0x3F

Base Address Selection

The module selector switches corresponds to address bits A23 – A16 on the VME address bus. Turning a selector switch will set a group of four address bits corresponding to four VME address bits.

Table 1 - Base Address Selection

Switch Settings						Address Range
SW2			SW1			
A23	…	A20	A19	…	A16	
0			0			000000 – 00FFFF
5			5			550000 – 55FFFF
A			A			AA0000 – AAFFFF
F			F			FF0000 – FFFFFF

Input Signals

$f_{0\ CHANNEL1-4}$ GATE, f_1 GATE, FREQ STRB, and **f_0 IDLE IN** are NIM input signals. RF Power Trip signal (**RF TRIP IN**) is an analog signal with maximum input level of 5 volts.

Output Signals

Σ_{OUT} GATE and **f_0 IDLE OUT** are NIM output signals. **Σ_{OUT} GATE** outputs gated signal selected by the **RF SEL GATED** selector switch. **RF SEL GATED OUT** is a view port of the postgated analog signals. **RF SEL PREGATED OUT** is a view port of the pregated analog signals. **Σ_{OUT} RF** is the analog sum of **$f_{0\ CHANNEL1-4}$ OUT** and **f_1 OUT** signals. All analog output signals have a maximum output level of ±1.0 volts into 50 ohms.

Operating Modes

Single Tone Mode

In this mode the carrier is not modulated. Frequency data is read from the Frequency Sweep Data Memory in the case of the $f_{0\ CHANNEL\ 1\ -\ 4}$ and from the VME frequency register in the case of the reference channel f_1, f_{C0} and f_{C1}. Since the $f_{0\ CHANNEL\ 1\ -\ 4}$ data is from the Frequency Sweep Data Memory at least one **FREQ STRB** strobe must be issued. If more than one **FREQ STRB** strobe is issued then operation proceeds according to the Frequency Sweep Data Memory description below.

Quadrature Modulation Mode

In Quadrature Mode I and Q data is read from the I&Q Data Memory. Each channel has its own memory. If an unmodulated carrier is wanted then the I and Q data are set to constant values. There is a separate length register associated with each I&Q Data Memory. When the length is set to zero the last memory location is used as the source of the I and Q data resulting in modulation by a pair of constant values.

Single Frequency

Only the last location (IDLE) in the Frequency Sweep Data Memory is used and at least one **FREQ STRB** strobe must be issued.

Swept Frequency

One 32-bit word is read from the Frequency Sweep Data Memory for each **FREQ STRB** strobe issued starting at the current location.

Functional Blocks

Frequency Sweep Data Memory

The Frequency Sweep Data Memory has 2048×32-bit frequency values stored in MSB to LSB order as the address increases. The IDLE frequency word must always be initialized. When the sweep reaches the end of the memory as defined by the length register the pointer advances to the IDLE frequency or stops at the Nth frequency according to the setting of the End Sweep Control register. For the special case where the length is set to zero the pointer always points to the IDLE frequency.

I&Q Data Memory

The I&Q memory contains the I and Q modulation values stored in alternating locations in MSB to LSB order as the address increases. Each channel has its own memory with 2048×10-bit I&Q data pairs and its own length register. When the GATE signal for a channel goes to the inactive state, its memory pointer is set to the first location. If the GATE remains active for a period longer than the time it takes to read out the memory, as defined by the length register for that channel, then the pointer advances to the IDLE location or stops at the Nth location according to the setting of the End Sweep Control register. For the special case where the length is set to zero the pointer always points to the IDLE location and the data pair at that location is used.

In order to increase memory depth, a “buffer factor” N_C has been implemented. The N_C value sets a delay, based on a 20 MHz I&Q data sample rate, before incrementing the I&Q data memory address.

The I and Q data is in 2's complement format.

RF TRIP

The **Σ_{OUT} RF** to the RF amplifier is enabled by the **RF TRIP IN** input. An input from the RF detector exceeding the trip level is latched and disables the **Σ_{OUT} RF**. The trip latch must be cleared by writing to the RF Power Status/Trip register in order to enable the output. A trip will occur if no cable is connected to the input. The trip circuit can be effectively disabled by connecting a 50 ohm terminator in place of the external cable.

GATE Signals

Active levels on the **f_0 CHANNEL 1 - 4** and **f_1 GATE** signals enable the corresponding RF signals and, in Quadrature Modulation mode, enables the modulation. The modulation data pointer is reset whenever the gate is in the inactive state. Readout begins from the first word each time the gate goes active.

Limitations

Maximum frequency sweep strobe rate is 200kHz.

Maximum I&Q data sample rate is 20MHz.

Maximum N_C buffer factor is 4096.

The minimum RF trip threshold is approximately 115mV and the maximum is approximately 4.85V.

Table 2 – Memory Map

Address (HEX)	Reset Value (HEX)	Operation	Description	Size
FFFF C05A			RESERVED	
C058	XXXX	R	Temperature of FPGA	16 bits
C057	00	R	RESERVED	8 bits
C056	00	R/W	VME Module Reset	0 bits
C055	00	R/W	VME Module Operating Mode	1 bit
C054	00	R/W	RF Power Trip Status/Reset	1 bit
C053	80	R/W	RF Power Trip Threshold	8 bits
C052	00	R/W	RF Gated Output Select	3 bits
C051	00	R/W	RF Pregated Output Select	3 bits
C050	00	R/W	Anciliary I/O Control	4 bits
C04F	00	R/W	Anciliary Output	4 bits
C04E	0X	R	Anciliary Input	4 bits
C04C	0155	R/W	$f_{0\ \text{CHANNEL 1 - 4}}$ and f_1 Gate Control	10 bits
C04B	3F	R/W	End Sweep Control	6 bits
C04A	00	R/W	Frequency Sweep Internal Strobe	0 bits
C049	00	R/W	Frequency Sweep Address Reset	0 bits
C048	00	R/W	Frequency Sweep Address Preset	0 bits
C046	07FF	R	Frequency Sweep Address	11 bits
C044	0000	R/W	Frequency Sweep Length	11 bits
C040	00000000	R/W	f_{C1} Frequency Tuning Word	32 bits
C03C	00000000	R/W	f_{C0} Frequency Tuning Word	32 bits
C03A	0000	R	RESERVED	16 bits
C039	00	R/W	$f_{C0,1}$ Output Select	1 bit
C038	80	R/W	$f_{C0,1}$ Output Scale Factor	8 bits
C034	00000000	R/W	f_1 Frequency Tuning Word	32 bits
C032	0000	R	RESERVED	16 bits
C030	07FF	R	f_1 I & Q Data Memory Address	11 bits
C02E	0000	R/W	f_1 I & Q Data Memory Length	11 bits
C02C	0001	R/W	f_1 N_c Buffer Factor	12 bits
C02B	00	R	RESERVED	8 bits
C02A	80	R/W	f_1 Output Scale Factor	8 bits
C028	0000	R/W	f_1 Phase Modulation	16 bits
C026	07FF	R	$f_{0\ \text{CHANNEL 4}}$ I & Q Data Memory Address	11 bits
C024	0000	R/W	$f_{0\ \text{CHANNEL 4}}$ I & Q Data Memory Length	11 bits
C022	0001	R/W	$f_{0\ \text{CHANNEL 4}}$ N_c Buffer Factor	12 bits
C021	00	R	RESERVED	8 bits
C020	80	R/W	$f_{0\ \text{CHANNEL 4}}$ Output Scale Factor	8 bits
C01E	0000	R/W	$f_{0\ \text{CHANNEL 4}}$ Phase Modulation	16 bits

Table 2 – Con't

Address (HEX)	Reset Value (HEX)	Operation	Description	Size
C01C	07FF	R	$f_{0\ CHANNEL\ 3}$ I & Q Data Memory Address	11 bits
C01A	0000	R/W	$f_{0\ CHANNEL\ 3}$ I & Q Data Memory Length	11 bits
C018	0001	R/W	$f_{0\ CHANNEL\ 3}$ N_c Buffer Factor	12 bits
C017	00	R	RESERVED	8 bits
C016	80	R/W	$f_{0\ CHANNEL\ 3}$ Output Scale Factor	8 bits
C014	0000	R/W	$f_{0\ CHANNEL\ 3}$ Phase Modulation	16 bits
C012	07FF	R	$f_{0\ CHANNEL\ 2}$ I & Q Data Memory Address	11 bits
C010	0000	R/W	$f_{0\ CHANNEL\ 2}$ I & Q Data Memory Length	11 bits
C00E	0001	R/W	$f_{0\ CHANNEL\ 2}$ N_c Buffer Factor	12 bits
C00D	00	R	RESERVED	8 bits
C00C	80	R/W	$f_{0\ CHANNEL\ 2}$ Output Scale Factor	8 bits
C00A	0000	R/W	$f_{0\ CHANNEL\ 2}$ Phase Modulation	16 bits
C008	07FF	R	$f_{0\ CHANNEL\ 1}$ I & Q Data Memory Address	11 bits
C006	0000	R/W	$f_{0\ CHANNEL\ 1}$ I & Q Data Memory Length	11 bits
C004	0001	R/W	$f_{0\ CHANNEL\ 1}$ N_c Buffer Factor	12 bits
C003	00	R	RESERVED	8 bits
C002	80	R/W	$f_{0\ CHANNEL\ 1}$ Output Scale Factor	8 bits
C000	0000	R/W	$f_{0\ CHANNEL\ 1}$ Phase Modulation	16 bits
BFFF A000	XXXXXXXX	R/W	Frequency Sweep Data Memory	2048 x 32 bits
9FFF 8000	XXXX	R/W	f_1 I & Q Data Memory 2's Complement	4096 x 10 bits
7FFF 6000	XXXX	R/W	$f_{0\ CHANNEL\ 4}$ I & Q Data Memory 2's Complement	4096 x 10 bits
5FFF 4000	XXXX	R/W	$f_{0\ CHANNEL\ 3}$ I & Q Data Memory 2's Complement	4096 x 10 bits
3FFF 2000	XXXX	R/W	$f_{0\ CHANNEL\ 2}$ I & Q Data Memory 2's Complement	4096 x 10 bits
1FFF 0000	XXXX	R/W	$f_{0\ CHANNEL\ 1}$ I & Q Data Memory 2's Complement	4096 x 10 bits

Memory areas between 0000h to BFFFh are uninitialized and not affected by VME resets.

Table 3 - Frequency Sweep and I&Q Data Memory Byte Order

Address	I&Q Data	Frequency Data
N+3	Q LSB	Byte 0 (LSB)
N+2	Q MSB	Byte 1
N+1	I LSB	Byte 2
N+0	I MSB	Byte 3 (MSB)

Register Description

$f_{0\ CHANNEL\ 1}$ Phase Modulation

ADDR	$xxxxC000 - C001															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R/W															
RESET	0															

Used to add a phase shift to $f_{0\ CHANNEL\ 1}$ RF signal when the module is in NQR mode.

$$\Phi_{f_{0\ CHANNEL\ 1}} = (360° \times f_{0\ CHANNEL\ 1}\ \text{Phase Modulation value}) \div 65536$$

A 0° phase shift is set for $f_{0\ CHANNEL\ 1}$ RF signal when the module is in NMR mode and this register is ignored.

$f_{0\ CHANNEL\ 1}$ Output Scale Factor

ADDR	$xxxxC002							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

$f_{0\ CHANNEL\ 1}$ N_C Buffer Factor

ADDR	$xxxxC004 - C005															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				1											

The 12-bit value sets the delay before incrementing the I&Q data memory address.

$$\text{delay} = f_{0\ CHANNEL\ 1}\ N_C \times 50\ \text{nsec}$$

$f_{0\ CHANNEL\ 1}$ I&Q Data Memory Length

ADDR	$xxxxC006 - C007															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

$f_{0\ CHANNEL\ 1}$ I&Q Data Memory Address

ADDR	$xxxxC008 - C009															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R										
RESET	0					$7FF										

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

$f_{0\ CHANNEL\ 2}$ Phase Modulation

ADDR	$xxxxC00A - C00B															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R/W															
RESET	0															

Used to add a phase shift to $f_{0\ CHANNEL\ 2}$ RF signal when the module is in NQR mode.

$$\Phi_{f_{0\ CHANNEL\ 2}} = (360° \times f_{0\ CHANNEL\ 2}\ \text{Phase Modulation value}) \div 65536$$

A 90° phase shift is set for $f_{0\ CHANNEL\ 2}$ RF signal when the module is in NMR mode and this register is ignored.

$f_{0\ CHANNEL\ 2}$ Output Scale Factor

ADDR	$xxxxC00C							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

$f_{0\ CHANNEL\ 2}$ N_C Buffer Factor

ADDR	$xxxxC00E - C00F															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				1											

The 12-bit value sets the delay before incrementing the I&Q data memory address.

$$delay = f_{0\ CHANNEL\ 2}\ N_C \times 50\ nsec$$

$f_{0\ CHANNEL\ 2}$ I&Q Data Memory Length

ADDR	$xxxxC010 - C011															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

$f_{0\ CHANNEL\ 2}$ I&Q Data Memory Address

ADDR	$xxxxC012 - C013															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R										
RESET	0					$7FF										

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

$f_{0\ CHANNEL\ 3}$ Phase Modulation

ADDR	$xxxxC014 - C015															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R/W															
RESET	0															

Used to add a phase shift to $f_{0\ CHANNEL\ 3}$ RF signal when the module is in NQR mode.

$$\Phi_{f_{0\ CHANNEL\ 3}} = (360° \times f_{0\ CHANNEL\ 3}\ \text{Phase Modulation value}) \div 65536$$

A 180° phase shift is set for $f_{0\ CHANNEL\ 3}$ RF signal when the module is in NMR mode and this register is ignored.

$f_{0\ CHANNEL\ 3}$ Output Scale Factor

ADDR	$xxxxC016							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

$f_{0\ CHANNEL\ 3}$ N_C Buffer Factor

ADDR	$xxxxC018 - C019															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				1											

The 12-bit value sets the delay before incrementing the I&Q data memory address.

$$\text{delay} = f_{0\ CHANNEL\ 3}\ N_C \times 50\ \text{nsec}$$

$f_{0\ CHANNEL\ 3}$ I&Q Data Memory Length

ADDR	$xxxxC01A - C01B															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

$f_{0\ CHANNEL\ 3}$ I&Q Data Memory Address

ADDR	$xxxxC01C - C01D															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R										
RESET	0					$7FF										

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

$f_{0\ CHANNEL\ 4}$ Phase Modulation

ADDR	$xxxxC01E - C01F															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R/W															
RESET	0															

Used to add a phase shift to $f_{0\ CHANNEL\ 4}$ RF signal when the module is in NQR mode.

$$\Phi_{f_{0\ CHANNEL\ 4}} = (360° \times f_{0\ CHANNEL\ 4}\ \text{Phase Modulation value}) \div 65536$$

A 270° phase shift is set for $f_{0\ CHANNEL\ 4}$ RF signal when the module is in NMR mode and this register is ignored.

$f_{0\ CHANNEL\ 4}$ Output Scale Factor

ADDR	$xxxxC020							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

$f_{0\ CHANNEL\ 4}$ N_C Buffer Factor

ADDR	$xxxxC022 - C023															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				1											

The 12-bit value sets the delay before incrementing the I&Q data memory address.

$$\text{delay} = f_{0\ CHANNEL\ 4}\ N_C \times 50\ \text{nsec}$$

$f_{0\ CHANNEL\ 4}$ I&Q Data Memory Length

ADDR	$xxxxC024 - C025															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

$f_{0\ CHANNEL\ 4}$ I&Q Data Memory Address

ADDR	$xxxxC026 - C027															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R										
RESET	0					$7FF										

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

f_1 Phase Modulation

ADDR	$xxxxC028 - C029															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R/W															
RESET	0															

Used to add a phase shift to f_1 RF signal.

$$\Phi_{f_1} = (360° \times f_1 \text{ Phase Modulation value}) \div 65536$$

f_1 Output Scale Factor

ADDR	$xxxxC02A							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

f_1 N_C Buffer Factor

ADDR	$xxxxC02C - C02D															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				1											

The 12-bit value sets the delay before incrementing the I&Q data memory address.

delay = f_1 N_C × 50 nsec

f_1 I&Q Data Memory Length

ADDR	$xxxxC02E - C02F															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

The 11-bit value is the number of valid I&Q data pairs stored in the I&Q Data Memory.

f_1 I&Q Data Memory Address

ADDR	$xxxxC030 - C031															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R										
RESET	0					$7FF										

The 11-bit value is the address pointer to the current I&Q data pair in the I&Q Data Memory. The default value points to the IDLE I&Q data pair.

f_1 Frequency Tuning Word

ADDR	$xxxxC034 - C037		
BIT	31	. . .	0
OPER	R/W		
RESET	0		

f_{OUT} = (Frequency Tuning Word × 200 ×10^6) ÷ 2^{32}

Frequency is updated once register $xxxxC037 (ie. Frequency Tuning Word LSB) is written.

$f_{C0,1}$ Output Scale Factor

ADDR	$xxxxC038							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit number that serves as a multiplier for the data pathway before data is delivered to the DAC. It has a LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

$f_{C0,1}$ Output Select

ADDR	$xxxxC039							
BIT	7	6	5	4	3	2	1	0
OPER	R							R/W
RESET	0							0

Sets the unmodulated frequency counter output available at the **FREQ COUNTER RF OUT** port.

bit 0: **0**: f_{C0} on view port
1: f_{C1} on view port.

f_{C0} Frequency Tuning Word

ADDR	$xxxxC03C - C03F		
BIT	31	. . .	0
OPER	R/W		
RESET	0		

$$f_{OUT} = (\text{Frequency Tuning Word} \times 200 \times 10^6) \div 2^{32}$$

Frequency is updated once register $xxxxC03F (ie. Frequency Tuning Word LSB) is written.

f_{C1} Frequency Tuning Word

ADDR	$xxxxC040 - C043		
BIT	31	. . .	0
OPER	R/W		
RESET	0		

$$f_{OUT} = (\text{Frequency Tuning Word} \times 200 \times 10^6) \div 2^{32}$$

Frequency is updated once register $xxxxC043 (ie. Frequency Tuning Word LSB) is written.

Frequency Sweep Length

ADDR	$xxxxC044 - C045															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

The 11-bit value is the number of valid 32-bit frequency tuning values stored in the Frequency Sweep memory.

Frequency Sweep Address

ADDR	$xxxxC046 - C047															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R										
RESET	0					$7FF										

The 11-bit value is the current address pointer into the Frequency Sweep memory. The default value points to the IDLE frequency.

Frequency Sweep Address Preset

ADDR	$xxxxC048							
BIT	7	6	5	4	3	2	1	0
OPER	R							
RESET	0							

Write cycle will preset Frequency Sweep Address pointer registers to the first frequency location. On the next FREQ STRB signal, the frequency at the first location will be loaded.

Frequency Sweep Address Reset

ADDR	$xxxxC049							
BIT	7	6	5	4	3	2	1	0
OPER	R							
RESET	0							

Write cycle will reset Frequency Sweep Address pointer registers to the default value and loads the IDLE frequency.

Frequency Sweep Internal Strobe

ADDR	$xxxxC04A							
BIT	7	6	5	4	3	2	1	0
OPER	R							
RESET	0							

Write cycle will load $\mathbf{f_{0\ CHANNEL\ 1-4}}$ with the frequency pointed to by the Frequency Sweep Address register.

End Sweep Control

ADDR	$xxxxC04B							
BIT	7	6	5	4	3	2	1	0
OPER	R		R/W					
RESET	0		$3F					

bits 7 - 6: ***Reserved***
bit 5: ***Frequency Sweep End Sweep Mode***
bit 4: ***f_1 I&Q End Sweep Mode***
bit 3: ***$f_{0\ CHANNEL\ 4}$ I&Q End Sweep Mode***
bit 2: ***$f_{0\ CHANNEL\ 3}$ I&Q End Sweep Mode***
bit 1: ***$f_{0\ CHANNEL\ 2}$ I&Q End Sweep Mode***
bit 0: ***$f_{0\ CHANNEL\ 1}$ I&Q End Sweep Mode***

0: stop at Nth if strobes or gate exceed length
1: jump to IDLE if strobes or gate exceed length.

$f_{0\ CHANNEL\ 1-4}$ and f_1 Gate Control

ADDR	$xxxxC04C - C04D															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R						R/W									
RESET	0						$155									

bit 9 - 8: ***f_1 Gate Control***
bit 7 - 6: ***$f_{0\ CHANNEL\ 4}$ Gate Control***
bit 5 - 4: ***$f_{0\ CHANNEL\ 3}$ Gate Control***
bit 3 - 2: ***$f_{0\ CHANNEL\ 2}$ Gate Control***
bit 1 - 0: ***$f_{0\ CHANNEL\ 1}$ Gate Control***

00b: front panel gate input disabled
01b: normal mode (Default)
10b: gate pulse inverted
11b: front panel gate input ignored and internal gate always ON

Anciliary Input

ADDR	$xxxxC04E							
BIT	7	6	5	4	3	2	1	0
OPER	R				R			
RESET	0				0			

Reads the **ANCIL I/O 1 - 4** ports, when in input mode (set by register $xxxxC050).

bits 7 - 4: ***Reserved***
bit 3: ***Anciliary Input Channel 4***
bit 2: ***Anciliary Input Channel 3***
bit 1: ***Anciliary Input Channel 2***
bit 0: ***Anciliary Input Channel 1***

Anciliary Output

ADDR	$xxxxC04F							
BIT	7	6	5	4	3	2	1	0
OPER	R				R/W			
RESET	0				0			

Sets the **ANCIL I/O 1 - 4** ports, when in output mode (set by register $xxxxC050), to levels set in register.

bits 7 - 4: ***Reserved***
bit 3: ***Anciliary Output Channel 4***
bit 2: ***Anciliary Output Channel 3***
bit 1: ***Anciliary Output Channel 2***
bit 0: ***Anciliary Output Channel 1***

Anciliary I/O Control

ADDR	$xxxxC050							
BIT	7	6	5	4	3	2	1	0
OPER	R				R/W			
RESET	0				0			

Configures each **ANCIL I/O 1 - 4** ports to NIM inputs or NIM outputs.

bits 7 - 4: ***Reserved***
bit 3: ***Anciliary I/O Channel 4 Mode***
bit 2: ***Anciliary I/O Channel 3 Mode***
bit 1: ***Anciliary I/O Channel 2 Mode***
bit 0: ***Anciliary I/O Channel 1 Mode***

0: NIM input
1: NIM output

RF Pregated Output Select

ADDR	$xxxxC051							
BIT	7	6	5	4	3	2	1	0
OPER	R					R/W		
RESET	0					0		

Sets the **RF SEL PREGATED RF OUT** view port to 1 of 6 available pregated RF signals.

000b: $f_{0\ \text{CHANNEL 1}}$ selected (Default)
001b: $f_{0\ \text{CHANNEL 2}}$ selected
010b: $f_{0\ \text{CHANNEL 3}}$ selected
011b: $f_{0\ \text{CHANNEL 4}}$ selected
100b: f_1 selected
101b: Σ_{OUT} selected
110b: invalid; previous setting used
111b: invalid; previous setting used

RF Gated Output Select

ADDR	$xxxxC052							
BIT	7	6	5	4	3	2	1	0
OPER	R					R/W		
RESET	0					0		

Sets the **RF SEL GATED RF OUT** view port to 1 of 6 available postgated RF signals.

000b: $f_{0\ \text{CHANNEL 1}}$ selected (Default)
001b: $f_{0\ \text{CHANNEL 2}}$ selected
010b: $f_{0\ \text{CHANNEL 3}}$ selected
011b: $f_{0\ \text{CHANNEL 4}}$ selected
100b: f_1 selected
101b: Σ_{OUT} selected
110b: invalid; previous setting used
111b: invalid; previous setting used

RF Power Trip Threshold

ADDR	$xxxxC053							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	$80							

8-bit value determines the RF Power trip level.

V_{TRIP} = (5 volts × 8-bit value) ÷ 255

RF Power Status/Trip Reset

ADDR	$xxxxC054							
BIT	7	6	5	4	3	2	1	0
OPER	R							R
RESET	0							0

bit 0: ***RF Power Trip Indicator***
0: normal operation
1: Σ_{OUT} tripped

Write cycle will clear RF Power Trip latch.

VME Module Operating Mode

ADDR	$xxxxC055							
BIT	7	6	5	4	3	2	1	0
OPER	R							R/W
RESET	0							0

bit 0: ***Operating Mode***
0: NMR Mode
1: NQR Mode

Sets the operating mode of the module.

VME Module Reset

ADDR	$xxxxC056							
BIT	7	6	5	4	3	2	1	0
OPER	R							
RESET	0							

Write cycle will reset all VME registers. Memory locations will be unaffected.

FPGA Temperature

ADDR	$xxxxC058															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R															
RESET	XXXX															

This register contains the temperature of the FPGA (Stratix II IC). Temperature readings are taken every 500ms and are accurate to ±1°C.

Temperature (°C)	**Digital Output (Binary, 2's Complement)**	
	D15 – D3	**D2 – D0**
150	0,1001,0110,0000	000
125	0,0111,1101,0000	000
25	0,0001,1001,0000	000
0.0625	0,0000,0000,0001	000
0	0,0000,0000,0000	000
-0.0625	1,1111,1111,1111	000
-25	1,1110,0111,0000	000
-55	1,1100,1001,0000	000

Block Diagram of Module Operation